Semiconductor IC Design with MyChipStationX

A Practical Guide to Modern ASIC Design: From Theory to Tape-out

Selconn Co., Ltd.

June 11, 2026

Agenda

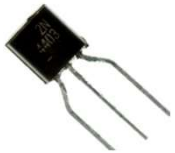
1. IC, Integrated Circuit
2. Basic Cell and it’s operation
3. Understanding IC design and production
4. About MyChipStationX
5. Basic Cell (Inverter) design example
6. Stopwatch design using MyChipStationX(Bottom-up)
7. About ASIC/SoC chipset design
8. Stopwatch design using MyChipStationX(Top-down)

SELCONN
SELECT & CONNECT

1. IC,Integrated Circuit

Semiconductor Device

Transistor, MOSFET, Resistor, Capacitor…

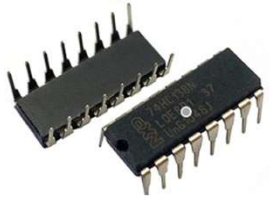


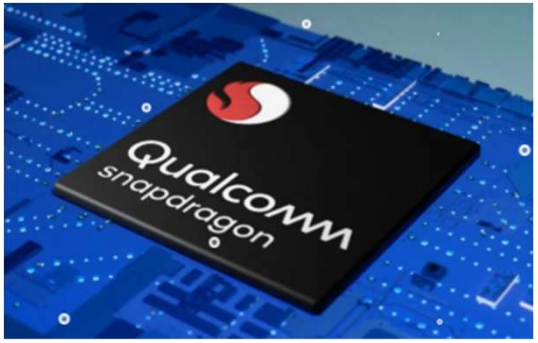

IC : IC is integrated circuit, many devices(transistors, resistors, capacitors…) is integrated on one chip (IC, ASIC, SoC…)

IC : Integrated Circuit

ASIC : Application Specific IC

SoC : System on Chip



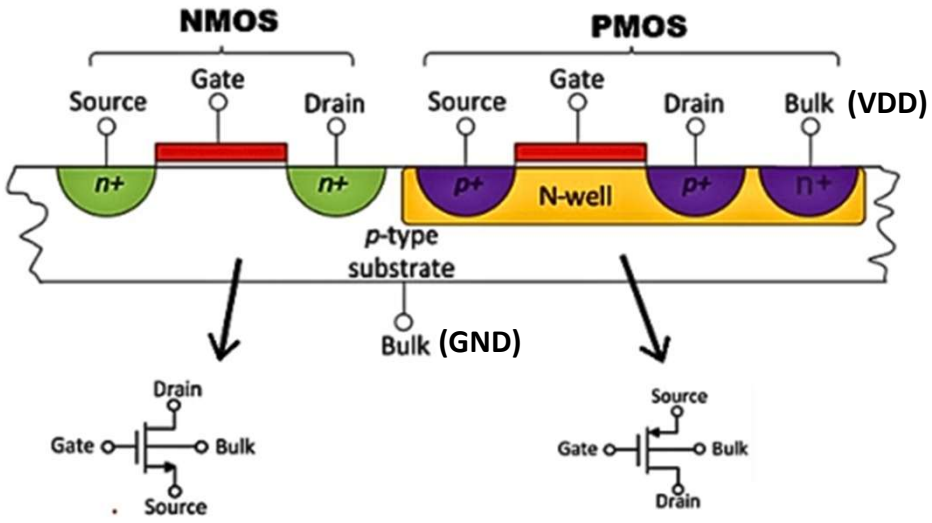


SELCONN
SELECT & CONNECT

2. Inverter Cell and operation of CMOS

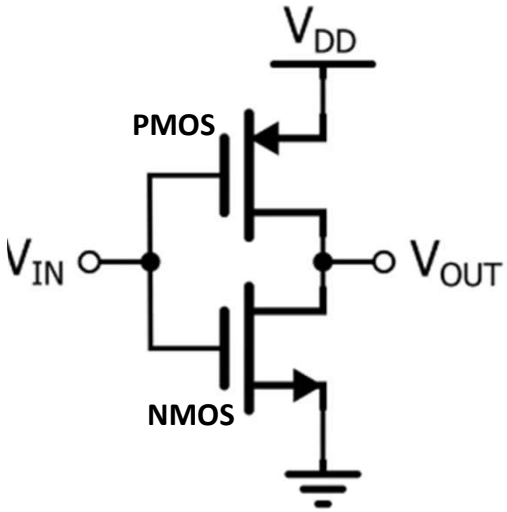
CMOS Device PMOS/NMOS
(Complementary Metal-Oxide-Semiconductor)

Wafer cross section



Gate width (channel length) is important.
Matured technology : 65/90/130/180/350/500nm

Inverter



VIN	VOUT
0	1
1	0

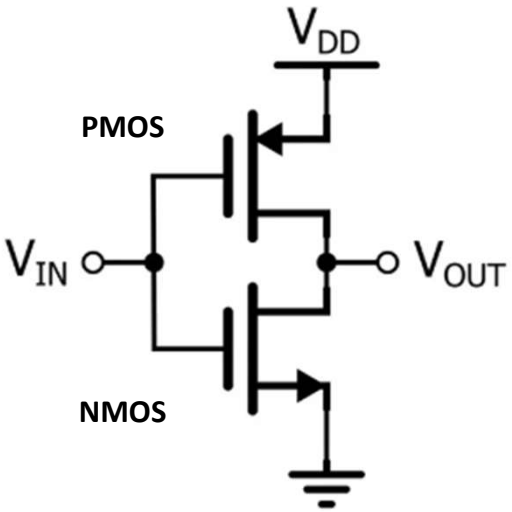
PMOS Operating Principle
When the gate voltage is low (ON)
•The gate is at a lower voltage than the n-well.
•A hole channel forms at the surface of the n-well.
•Current flows (Source → Drain).
When the gate voltage is high (OFF)
•No channel is formed.
•Current flow is blocked.

NMOS Operating Principle
When the gate voltage is low (OFF)
•No channel is formed.
•Current flow is blocked.
When the gate voltage is high (ON)
•The gate is at a higher voltage than the p-substrate.
•An electron channel forms at the surface of the p-substrate.
•Current flows (Drain → Source).

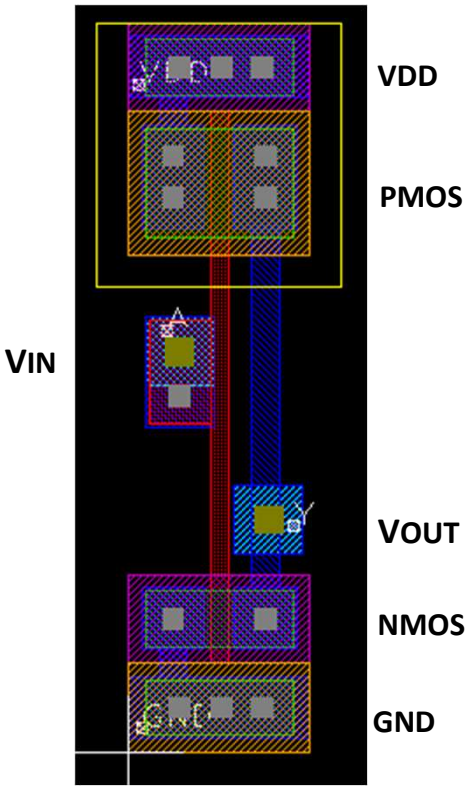
SELCONN
SELECT & CONNECT

2. Inverter Cell and operation of CMOS

Inverter



Cell(Wafer) 평면



PMOS Operating Principle

When the gate voltage is low (ON)

•The gate is at a lower voltage than the n-well.

•A hole channel forms at the surface of the n-well.

•Current flows (Source → Drain).

When the gate voltage is high (OFF)

•No channel is formed.

•Current flow is blocked.

NMOS Operating Principle

When the gate voltage is low (OFF)

•No channel is formed.

•Current flow is blocked.

When the gate voltage is high (ON)

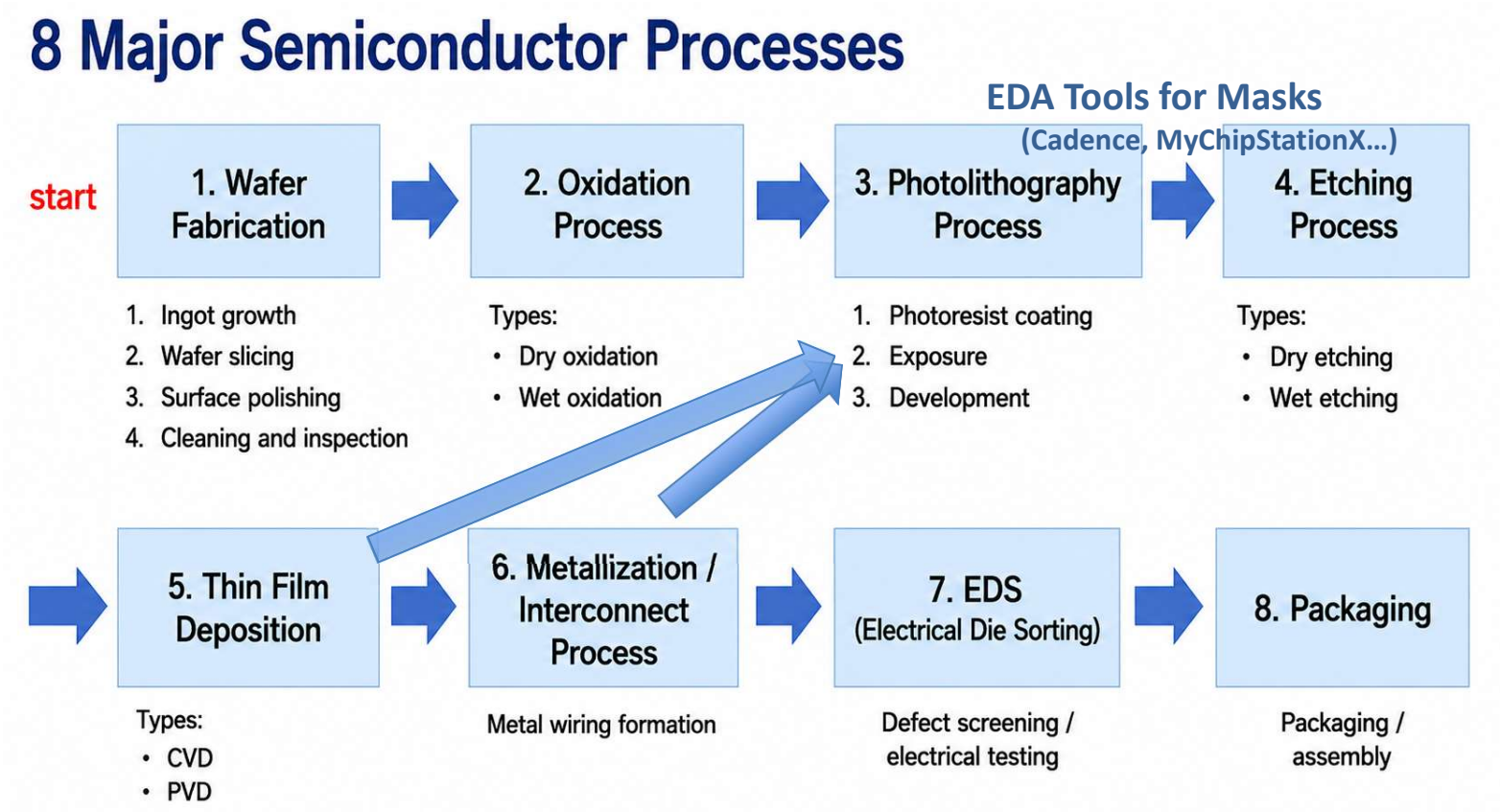
•The gate is at a higher voltage than the p-substrate.

•An electron channel forms at the surface of the p-substrate.

•Current flows (Drain → Source).

SELCONN
SELECT & CONNECT

3. Understanding IC design and production

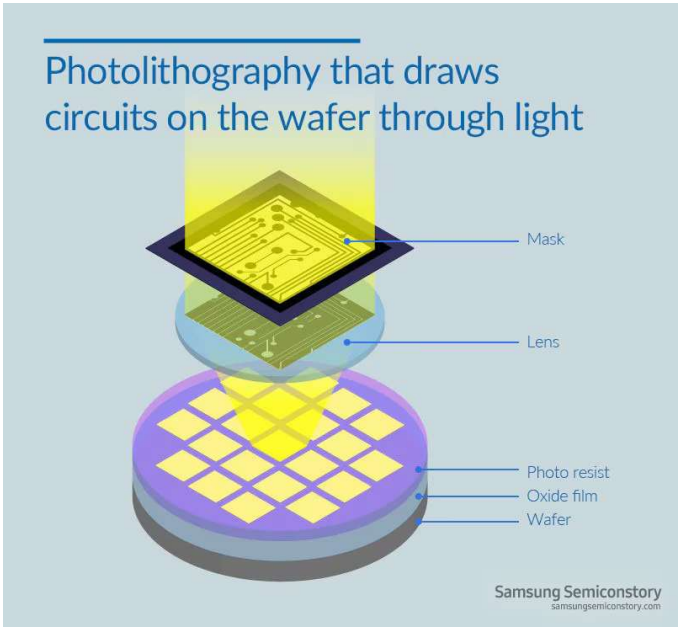


SELCONN
SELECT & CONNECT

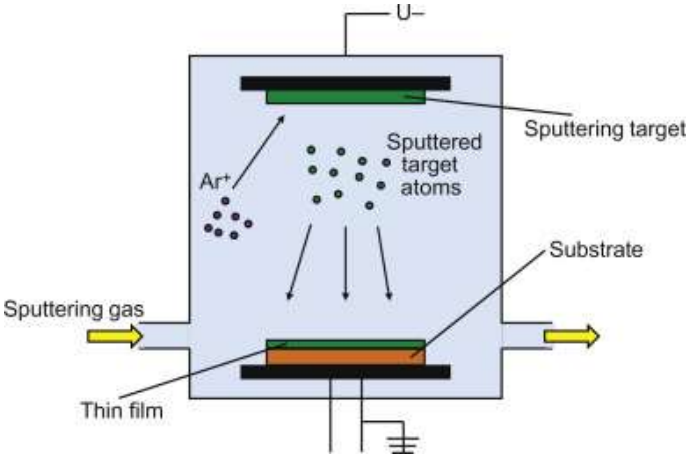
3. Understanding IC design and production

Some examples of semiconductor fabrication Process

Ingot/Wafer



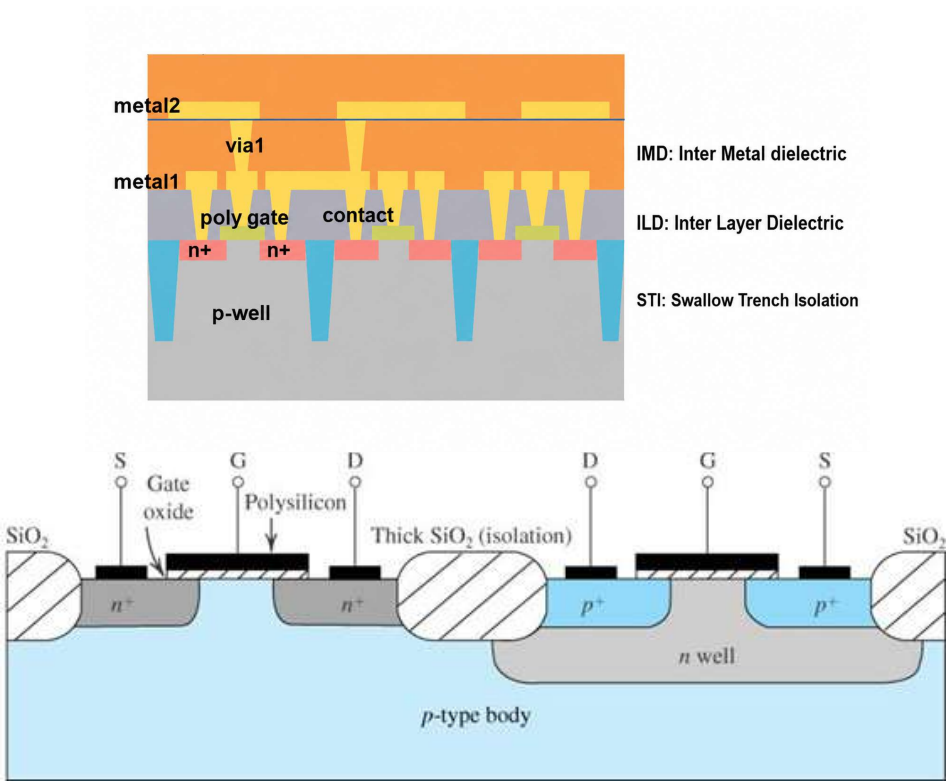
Photolithography



Physical Vapor Deposition

SELCONN
SELECT & CONNECT

3. Understanding IC design and production



The purpose of EDA tools is to create accurate masks required for the semiconductor manufacturing process.

CMOS Fabrication Flow

1. Wafer Preparation

•Start with a silicon wafer

•Form the initial oxide layer

2. Isolation Formation (Active Mask / STI)

•Define active regions

•Form **STI (Shallow Trench Isolation)** by filling non-active regions with oxide

•**PR coating → Exposure → Development → Etching / Oxide fill**

3. Well Formation

•Form **n-well** and/or **p-well** regions using well masks

•**PR coating → Exposure → Development → Ion implantation + Annealing**

4. Gate Oxide Growth

•Grow a thin gate oxide layer

5. Polysilicon Deposition

•Deposit a polysilicon layer for gate formation

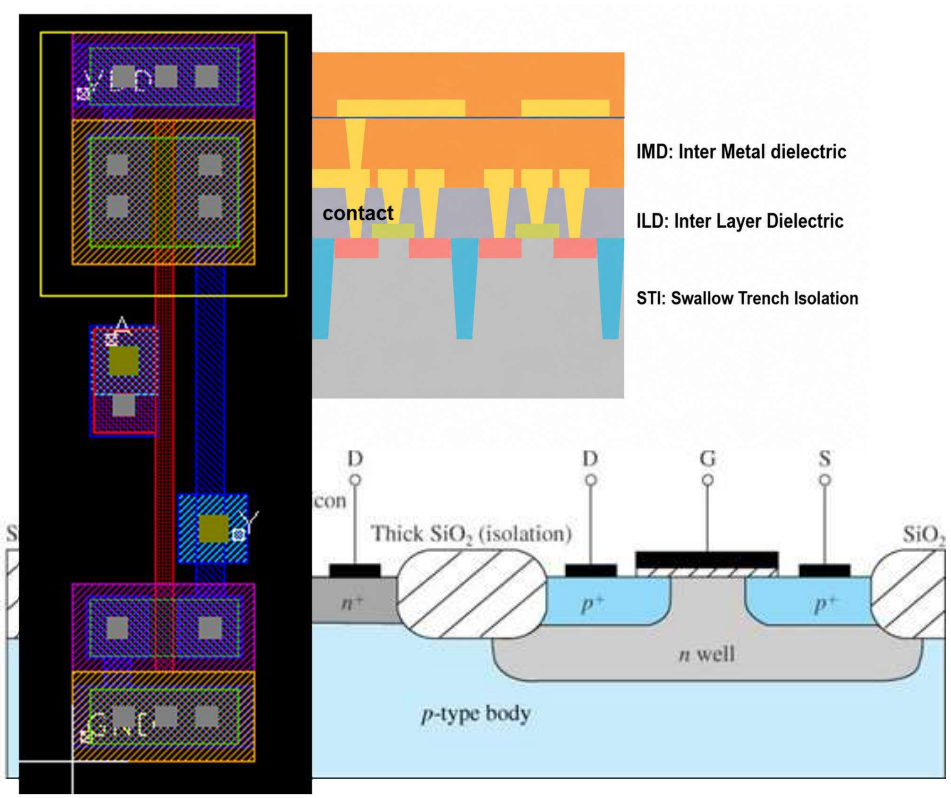
6. Gate Formation (Poly Mask)

•Pattern the polysilicon gate

•**PR coating → Exposure → Development → Etching**

SELCONN
SELECT & CONNECT

3. Understanding IC design and production



The purpose of EDA tools is to create accurate masks required for the semiconductor manufacturing process.

CMOS Fabrication Flow (Continue)

7. Source/Drain Formation

•Define source/drain regions using implant masks

•PR coating → Exposure → Development

•LDD implantation → Spacer formation → Heavy source/drain implantation

8. Interlayer Dielectric (ILD) Deposition

•Deposit the ILD layer

9. Contact Formation (Contact Mask)

•Open contact holes to source/drain and gate regions

•PR coating → Exposure → Development → Etching

10. Contact Fill

•Fill contact holes with a conductive material such as **tungsten**

11. Metal Interconnect Formation (Metal Mask)

•Deposit the metal layer

•Pattern interconnects using photolithography and etching

•Metal deposition → PR coating → Exposure → Development → Etching

12. Passivation / Final Processing

•Deposit the passivation layer for protection

•Complete final testing and packaging

SELCONN
SELECT & CONNECT

3. Understanding IC design and production

Process Design Kit(PDK)

ETRI 서울대학교 DGIST

2. Layer Information

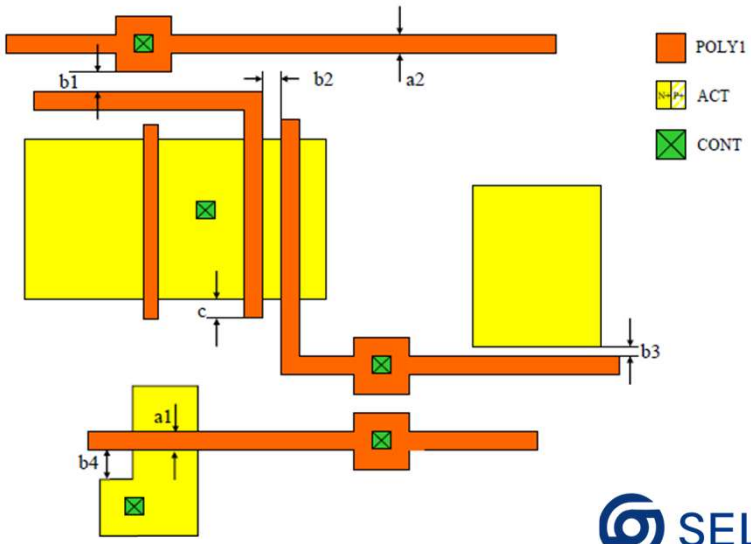
2.1 Layers for Standard Process

Layer Name	Layer No.	Function	Digitized Area
CHIPBOUNDARY	0	Define chip boundary	C
KEY	1	Define Align key	C
NWELL	2	Define N-well for PMOS body	C
PWELL	3	Define P-well for NMOS body	C
ACT	11	Define Active area	D
POLY1	12	Define Poly-Si 1 for gate of transistor	D
POLY2	13	Define Poly-Si 2 for resistor and capacitor	D
NSD	14	Define N-type implant region for N-LDD and N+	C
PSD	15	Define N-type implant region for P-LDD and P+	C
ESDI	26	Define ESD implant	C
CONT	31	Define contact from MET1 to ACT, POLY1 and POLY2	C
MET1	32	Define Metal-1 for interconnection	D
VIA1	33	Define Via1 connecting MET1 and MET2	C
MET2	34	Define Metal-2 for interconnection	D
VIA2	35	Define Via2 connecting MET2 and MET3	C
MET3	36	Define Metal-3 for interconnection	D
PAD	37	Define open region of passivation for bonding pad	C

4.3 POLY1 Rules

ETRI 500nm FAB (Poly1 width > 500nm)

Rule No.	Description	Label		Value (μm)
3.PL1.W1	POLY1 width over ACT (NMOS or PMOS)	a1	≥	0.5
3.PL1.W2	Maximum POLY1 width (Transistor Channel Length)	a1	≤	100.0
3.PL1.W3	POLY1 width for interconnect	a2	≥	0.5
3.PL1.S1	POLY1 to POLY1 space in field	b1	≥	0.6
3.PL1.S2	POLY1 to POLY1 space on ACT	b2	≥	0.6
3.PL1.S3	Space from POLY1 in field to ACT	b3	≥	0.5
3.PL1.S4	ACT space to POLY1 in field	b4	≥	0.5
3.PL1.O	Overlap of POLY1 extended into field oxide	c	≥	0.5
3.PL1.ANT	Maximum ratio of field poly area to gate poly for a given transistor(antenna rule)		≤	200

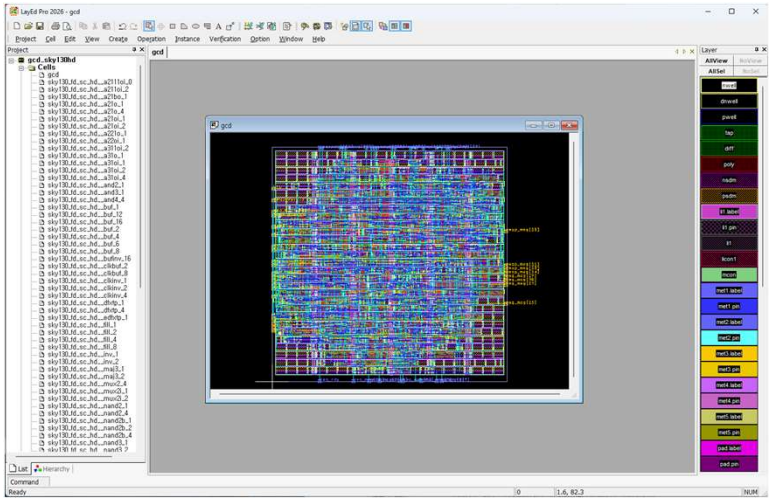


SELCONN
SELECT & CONNECT

4. MyChipStationX - introduction

MyChipStationX is a modernized semiconductor design platform developed by Selconn, based on proven MyCAD technology heritage dating back to 1990 and worldwide deployment across industrial, academic, and research environments.

- A complete EDA environment for analog/digital IC design
- Layout editing and verification (DRC/ERC/LVS/PEX)



SchedPro : Schematic Capture
Logic2Spice : Schematic to Spice netlist conversion

LayEdPro : MyChipStationX main program including Layout Editor
CifGdsPro : File format converter, including GDSII import/export
MyDRCPro : Design rule checking(FAB specific)
LayNetPro : ERC checking & netlist extraction
MyLVSPro : Layout vs Schematic comparison

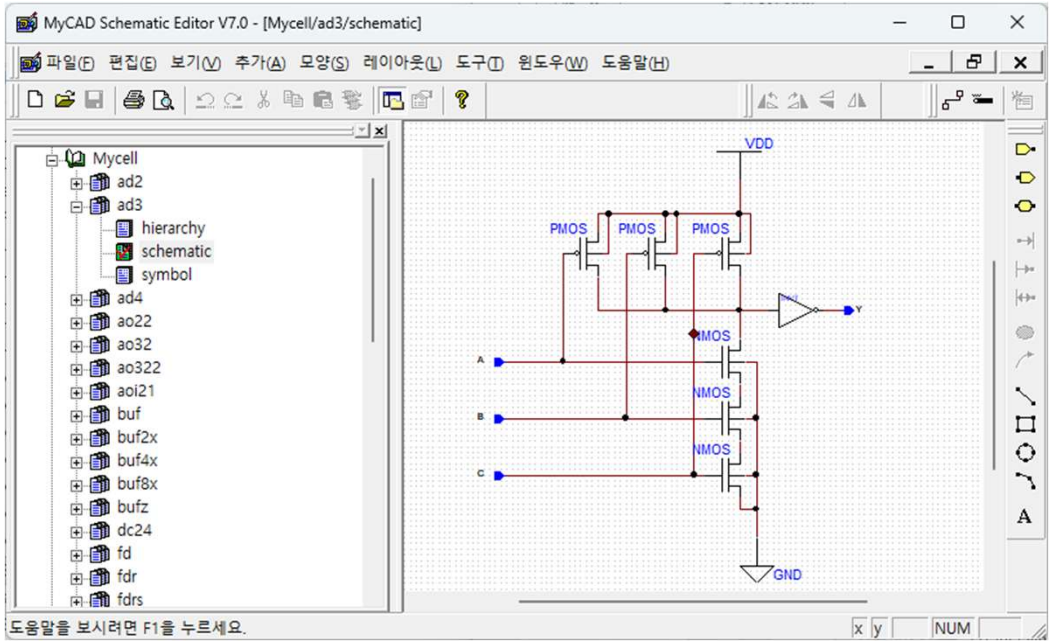
MyOpenROAD : OpenROAD (open-source Synthesis & PnR tool) Launcher

*GDSII (Graphic Data System II): Final layout file for photomask generation.)

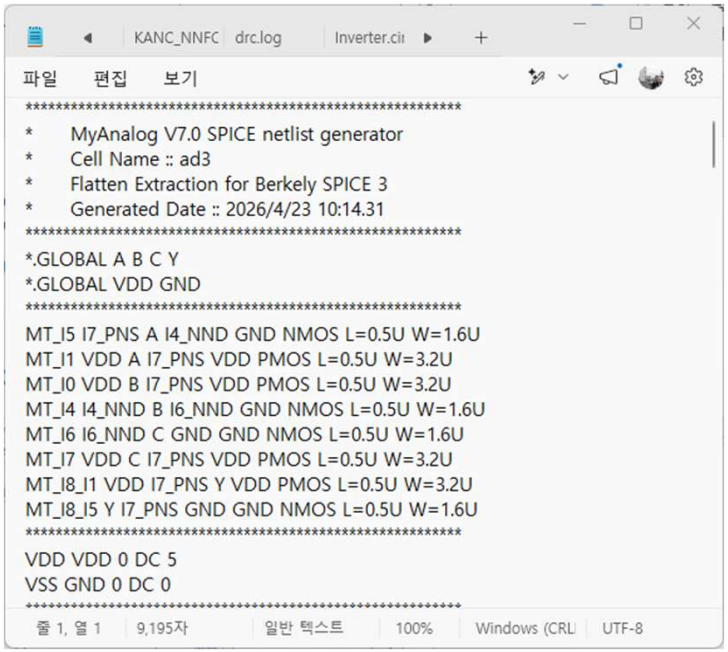
SELCONN
SELECT & CONNECT

4. MyChipStationX – Schematic Capture

SchedPro : Schematic Editor/Capture
Logic2Spice : Schematic to Spice netlist conversion



AND3 Schematic

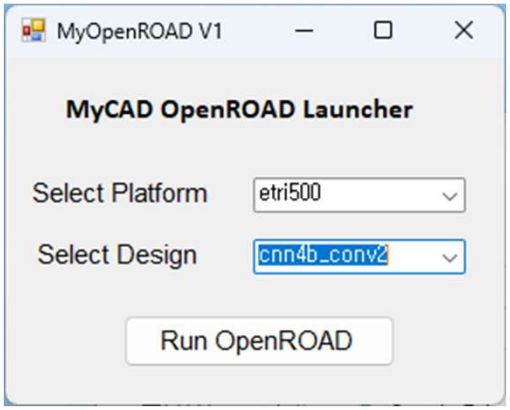


Netlist of AND3

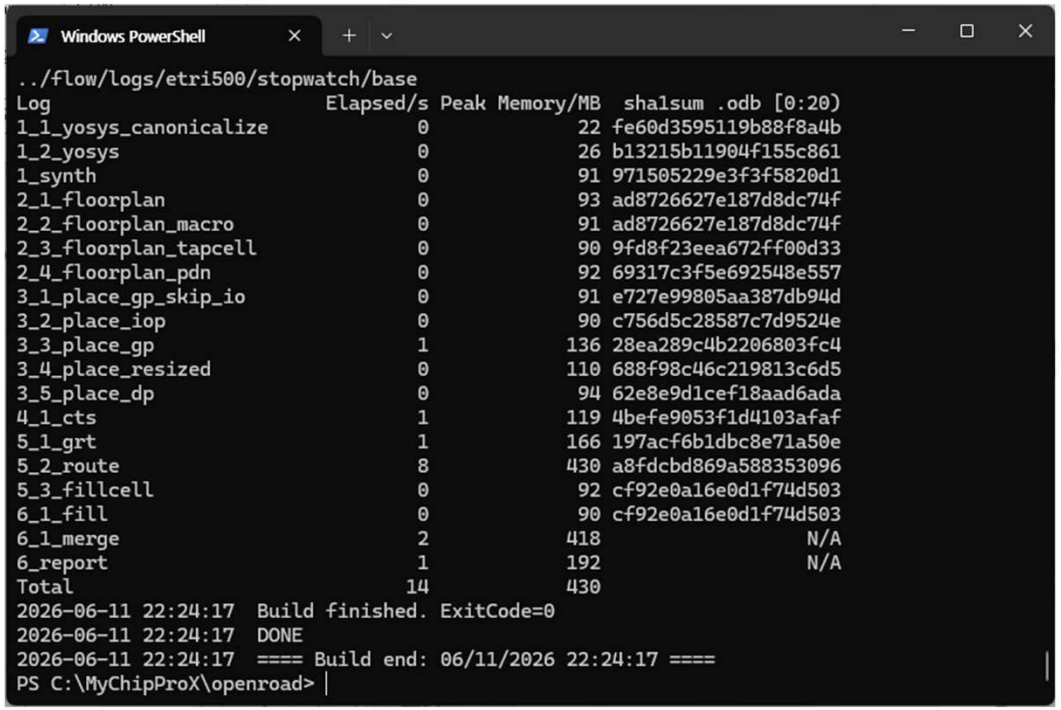
SELCONN
SELECT & CONNECT

4. MyChipStationX – Synthesis and PnR

MyOpenROAD.exe : OpenROAD launcher for synthesis and PnR



MyOpenROAD.exe

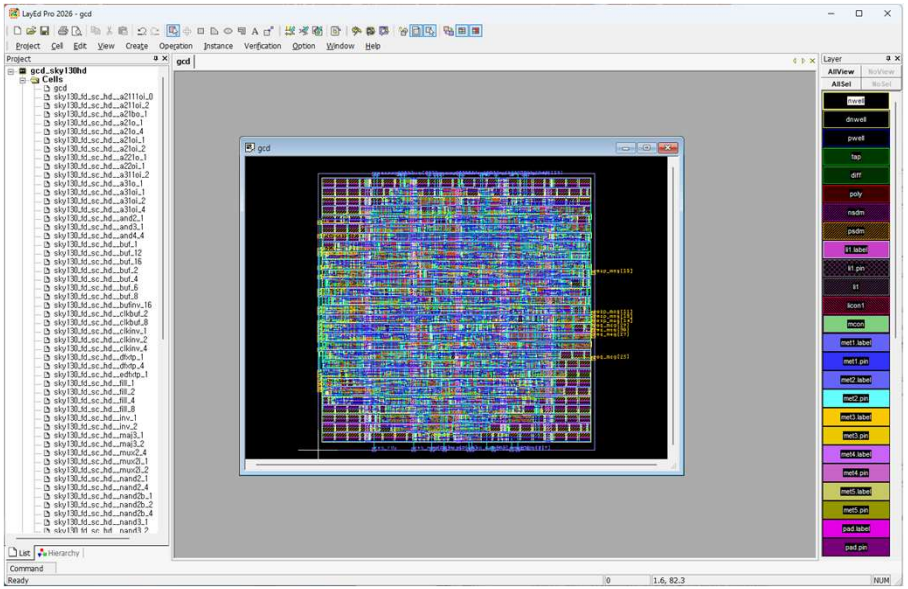


Result of OpenROAD

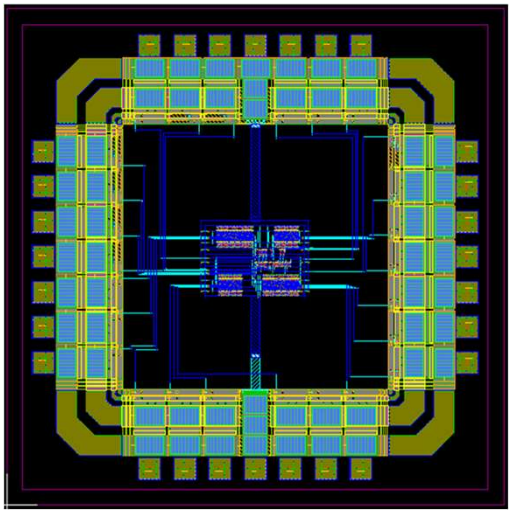
SELCONN
SELECT & CONNECT

4. MyChipStationX – Layout Editing

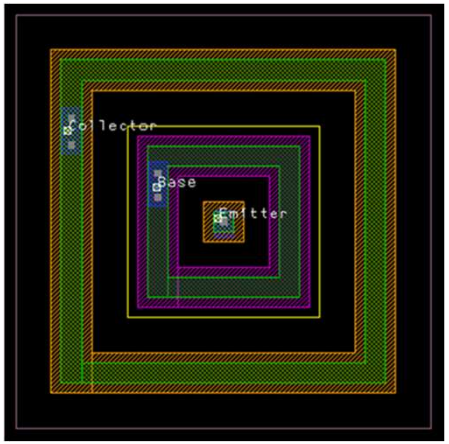
LayEdPro : Layout Editor
CifGdsPro : File format converter, including GDS import/export



Layout Viewer & Editor



Stopwatch core and IO PAD

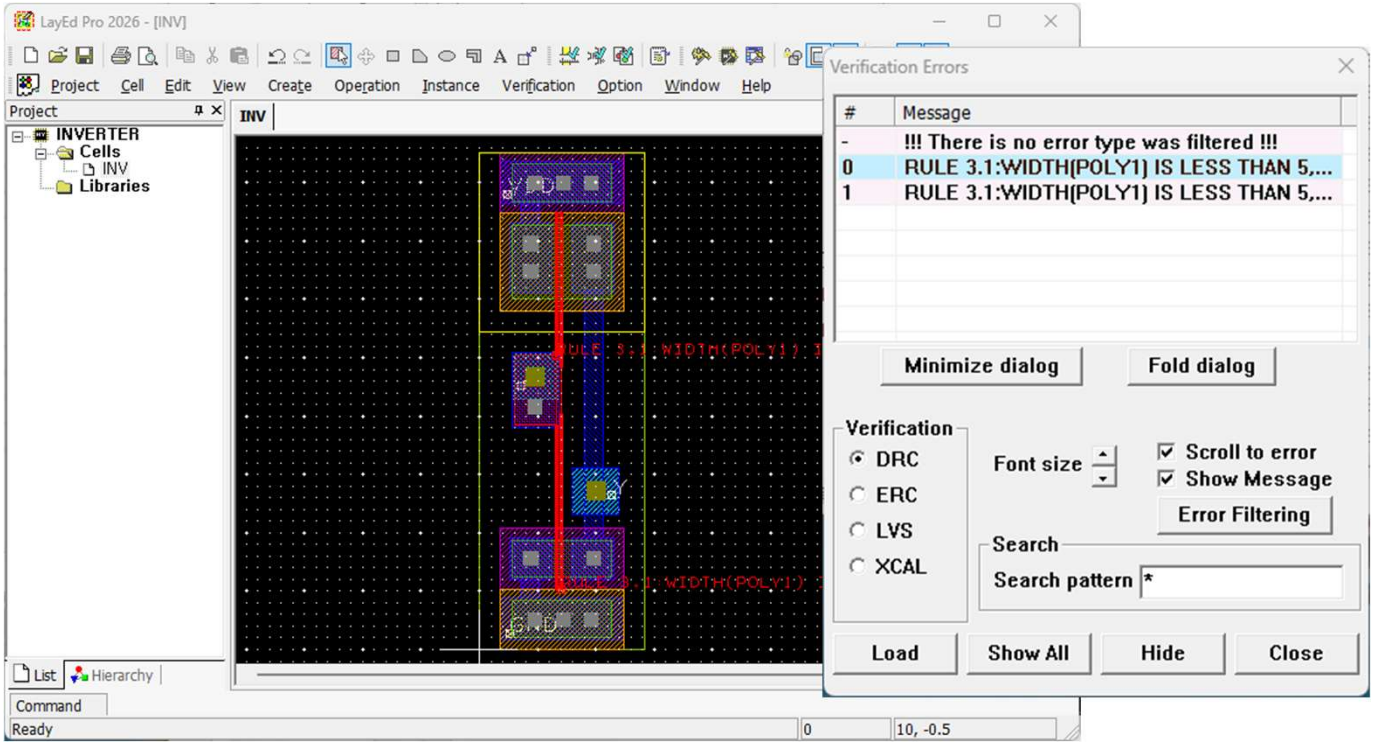


Bipolar Junction Transistor

SELCONN
SELECT & CONNECT

4. MyChipStationX - Verification

MyDRCPro : Design rule checking(FAB specific)

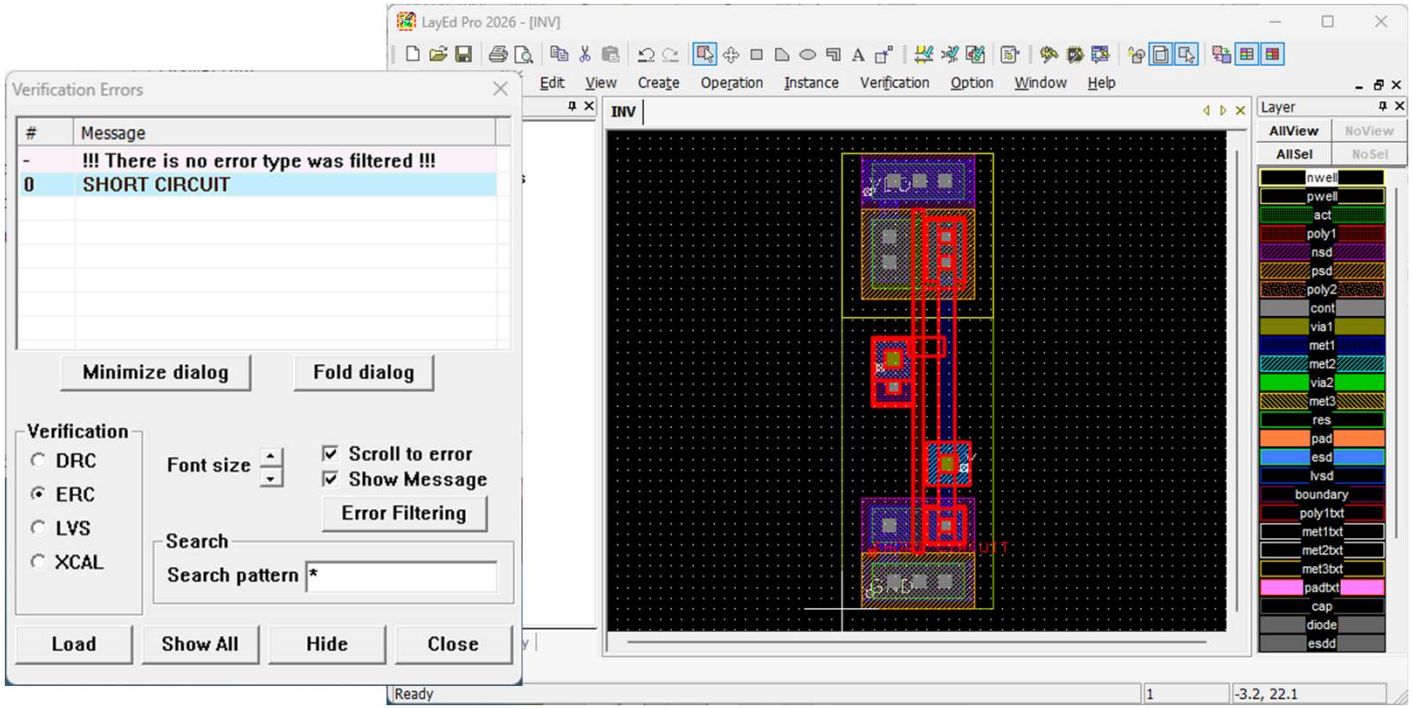


Design Rule Check result – 2 errors, poly1 width error (less than 500nm)

SELCONN
SELECT & CONNECT

4. MyChipStationX - Verification

MyERCPro : Electrical rule checking (Detection of Electrical Rule Violations)

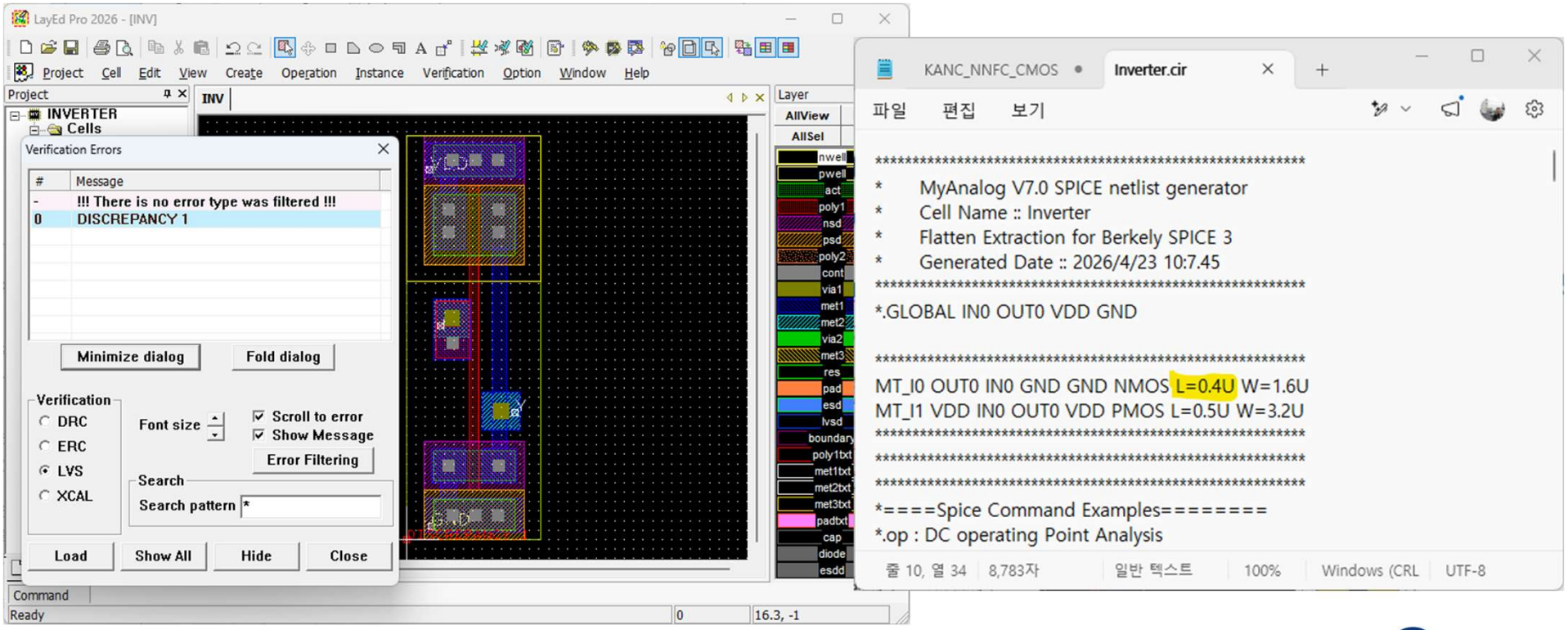


Electrical Rule Check result – 1 errors, short between input A and output Y

SELCONN
SELECT & CONNECT

4. MyChipStationX - Verification

MyLvsPro : Layout versus Schematic checking



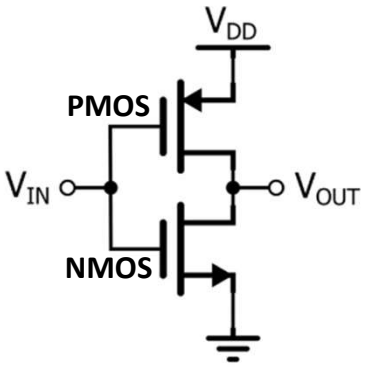
LVS Check result – 1 errors, discrepancy between NMOS Gate width in circuit and Layout gate width

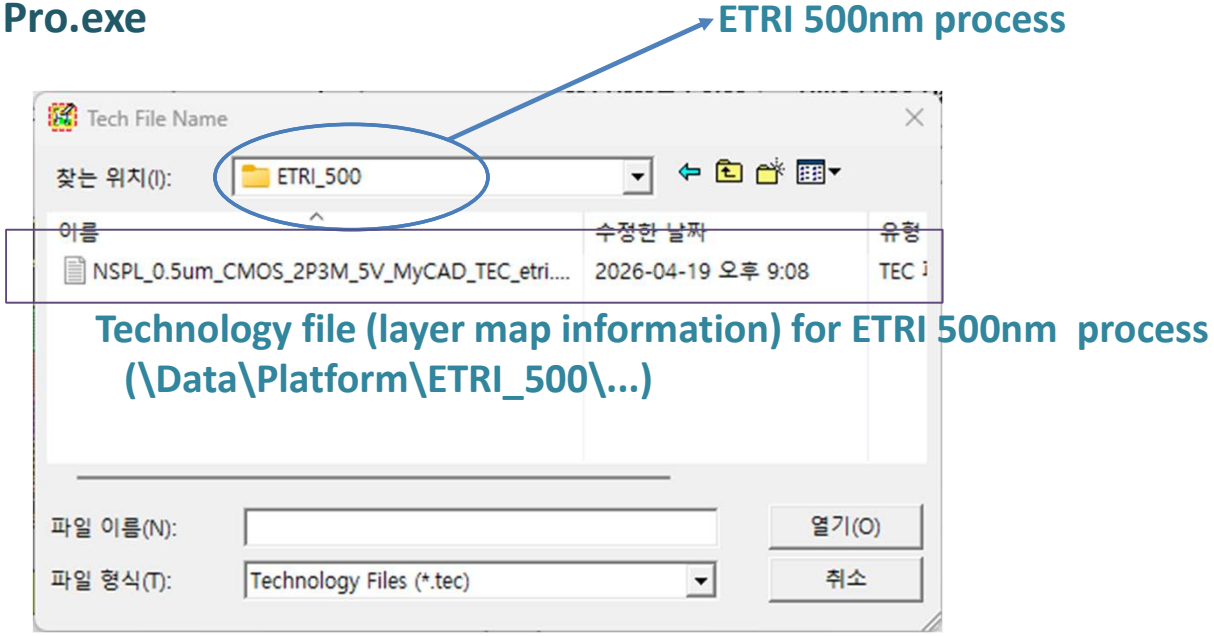
SELCONN
SELECT & CONNECT

5. Cell design example - Inverter

What You Need

1. Schematic
2. Platform PDK files (Technology, Rule, and Mapping Files for Semiconductor Fabrication)
3. Generating Project on LayEdPro.exe

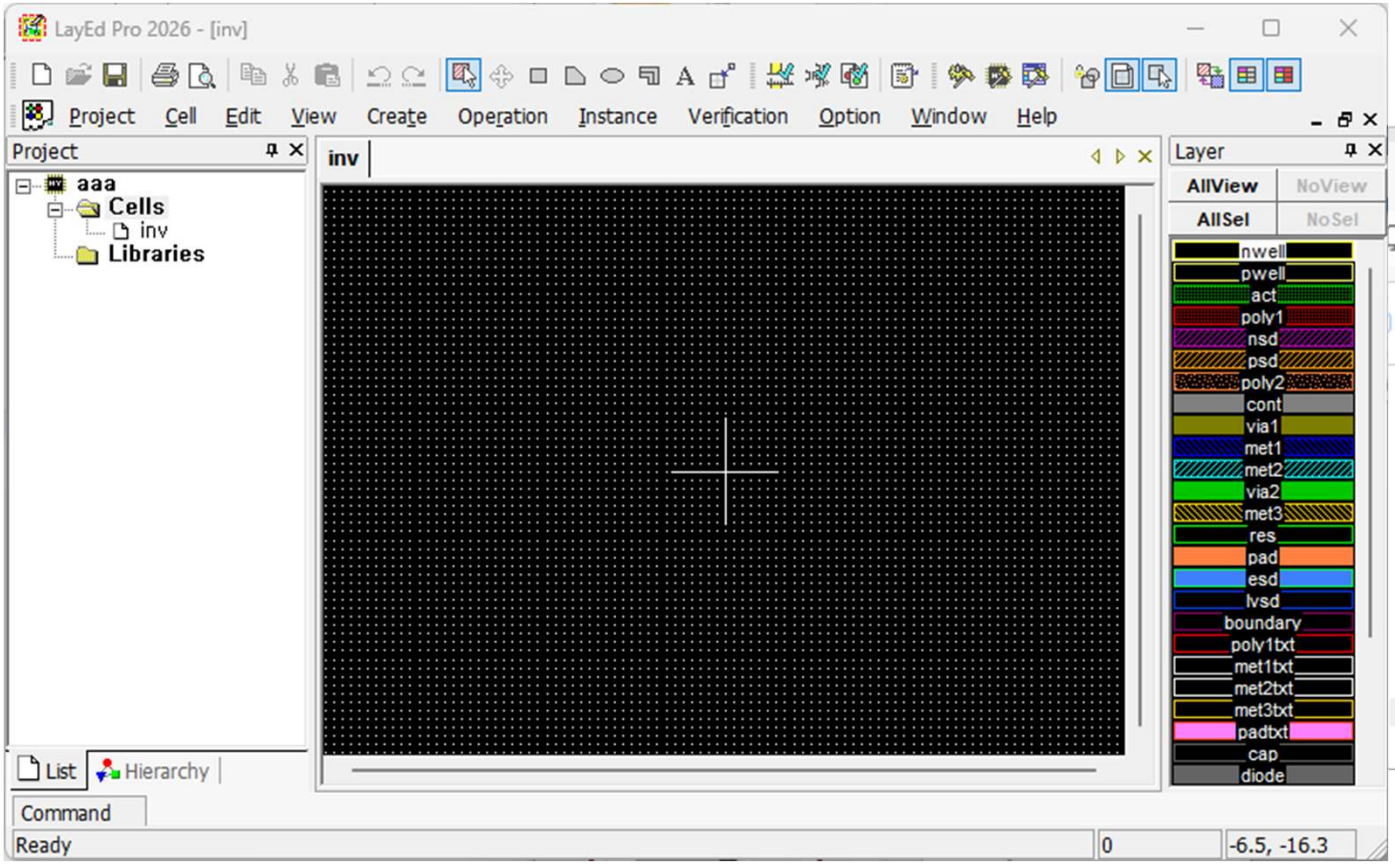


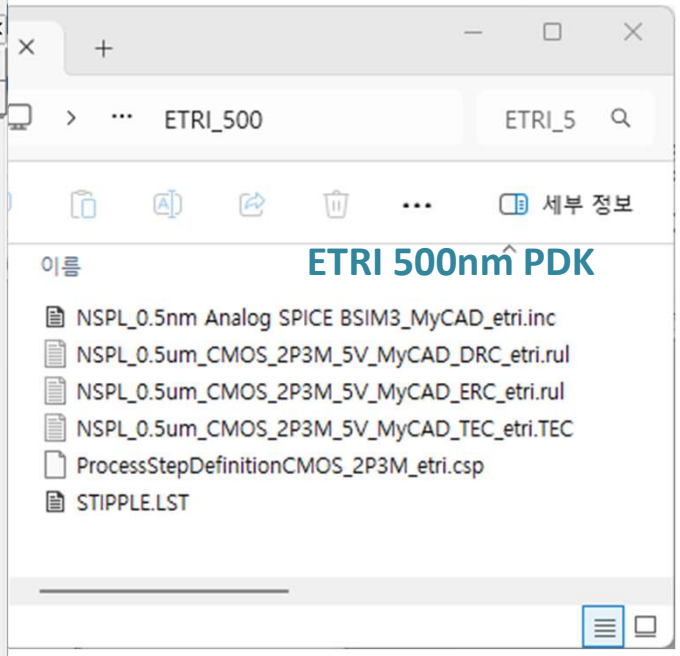


SELCONN
SELECT & CONNECT

5. Cell design example - Inverter

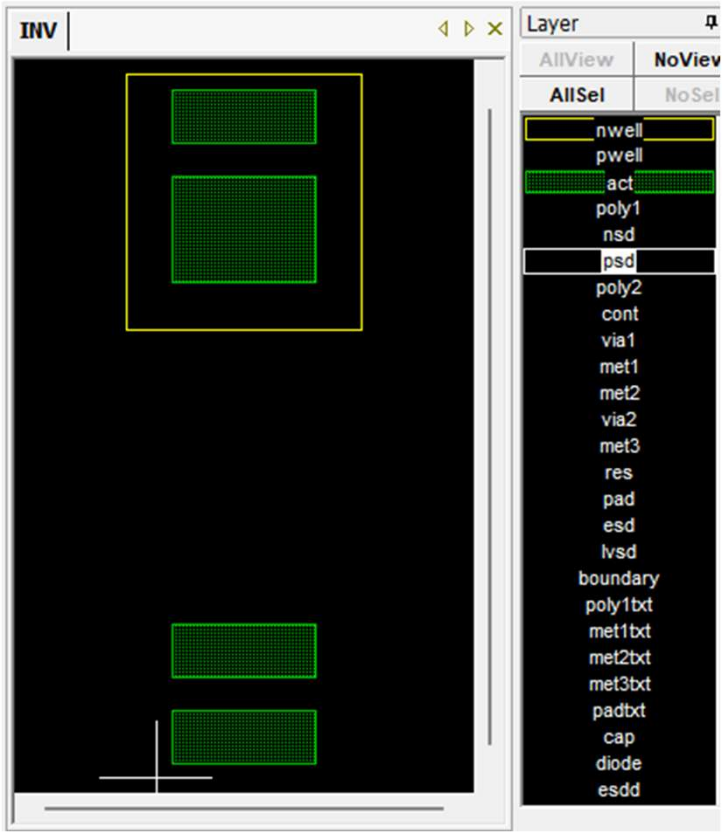
Ready for ETRI 500 process (Cell -> new cell -> generate ‘inv cell’)



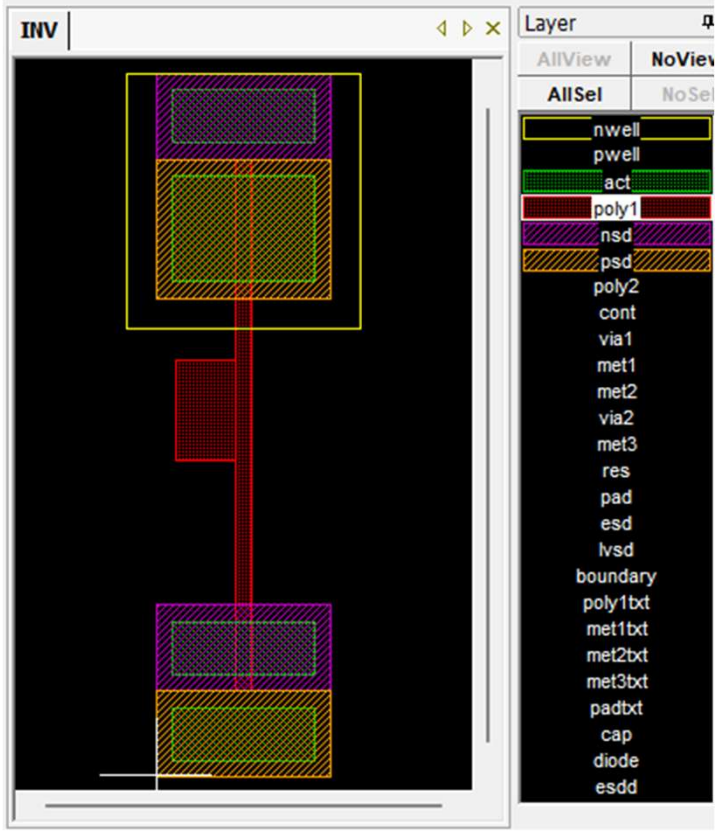


SELCONN
SELECT & CONNECT

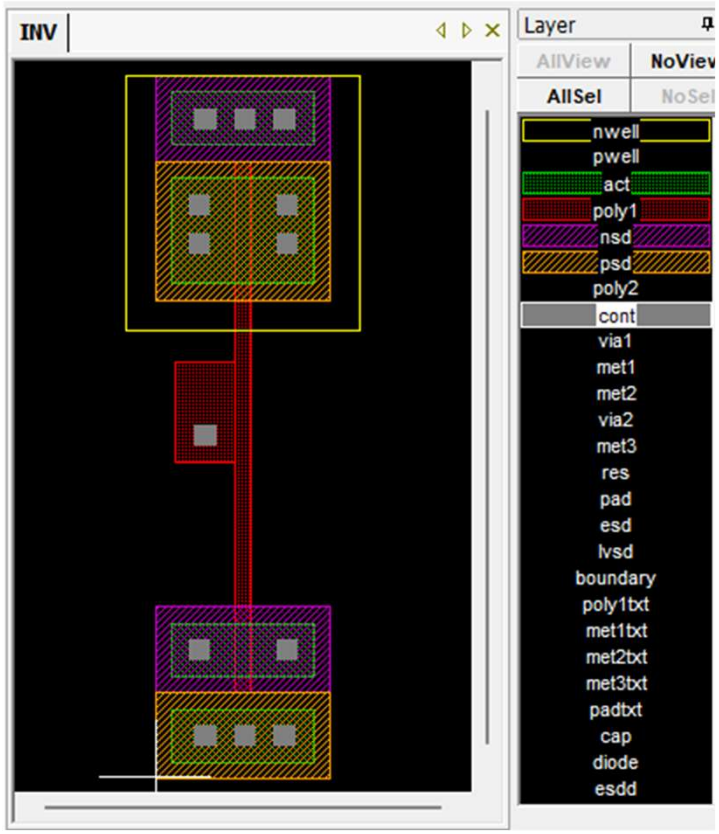
5. Cell design example - Inverter



n-welll/act



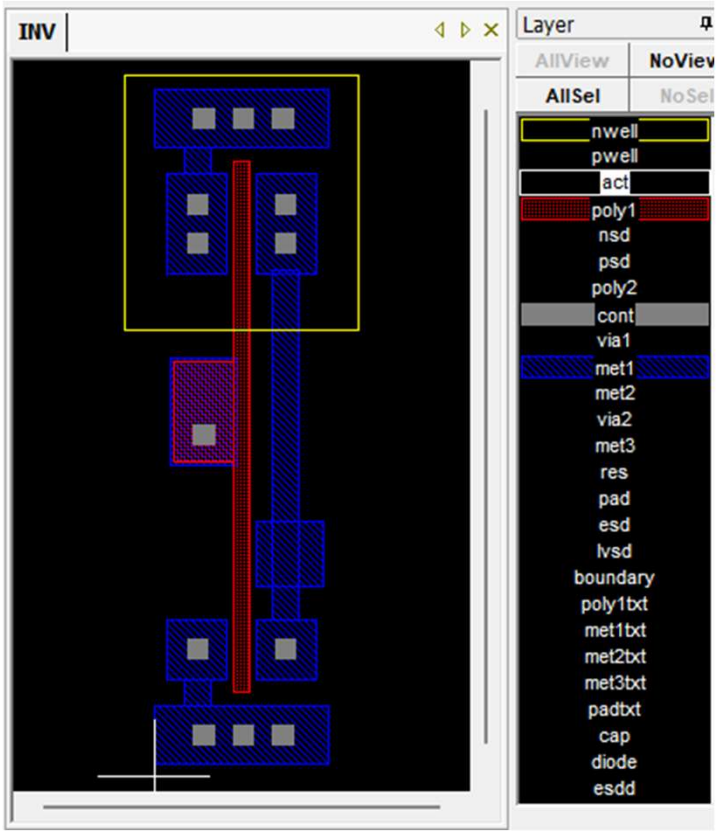
poly1/psd/nsd



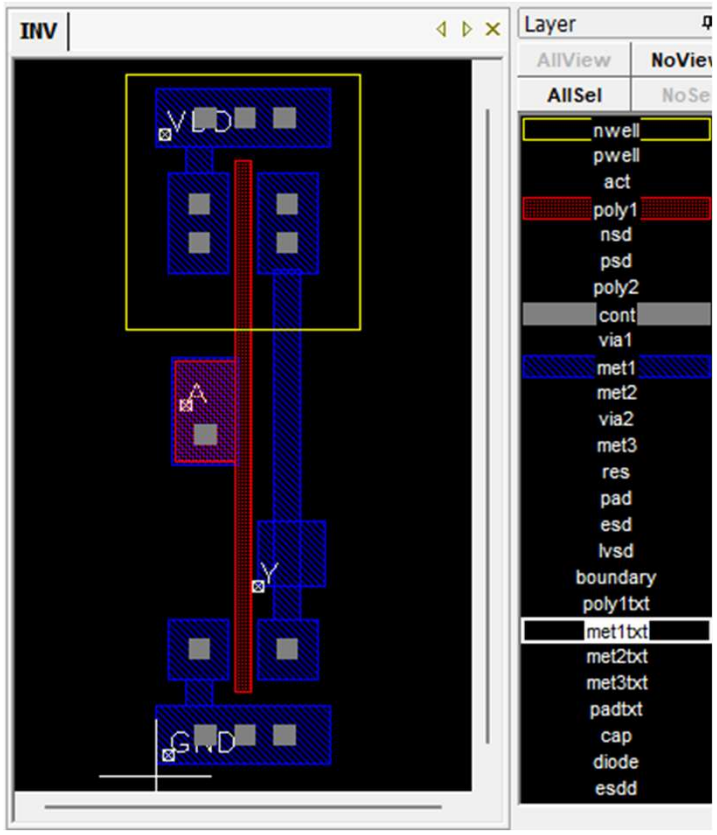
contact

SELCONN
SELECT & CONNECT

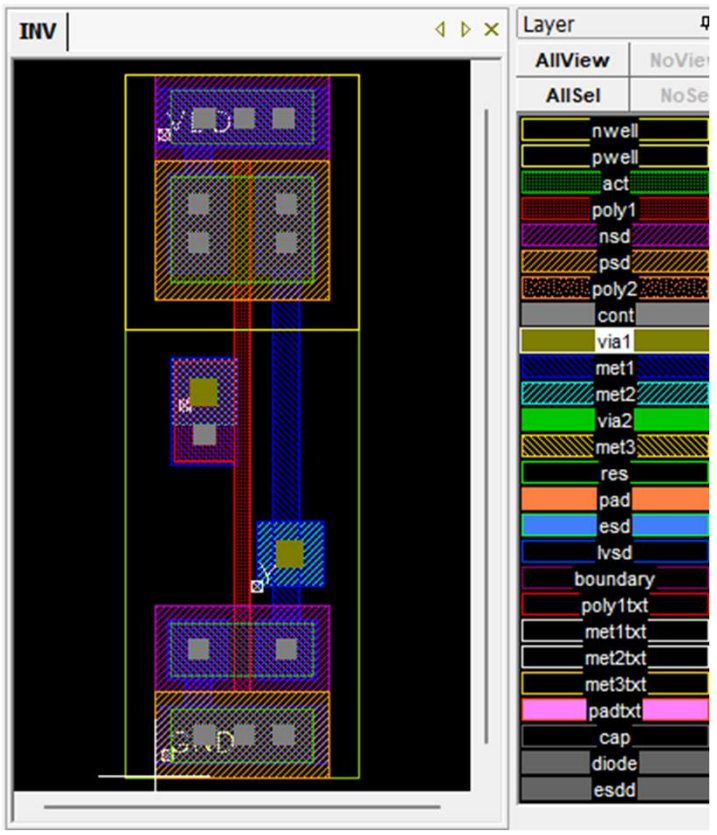
5. Cell design example - Inverter



metal1



text1(label)

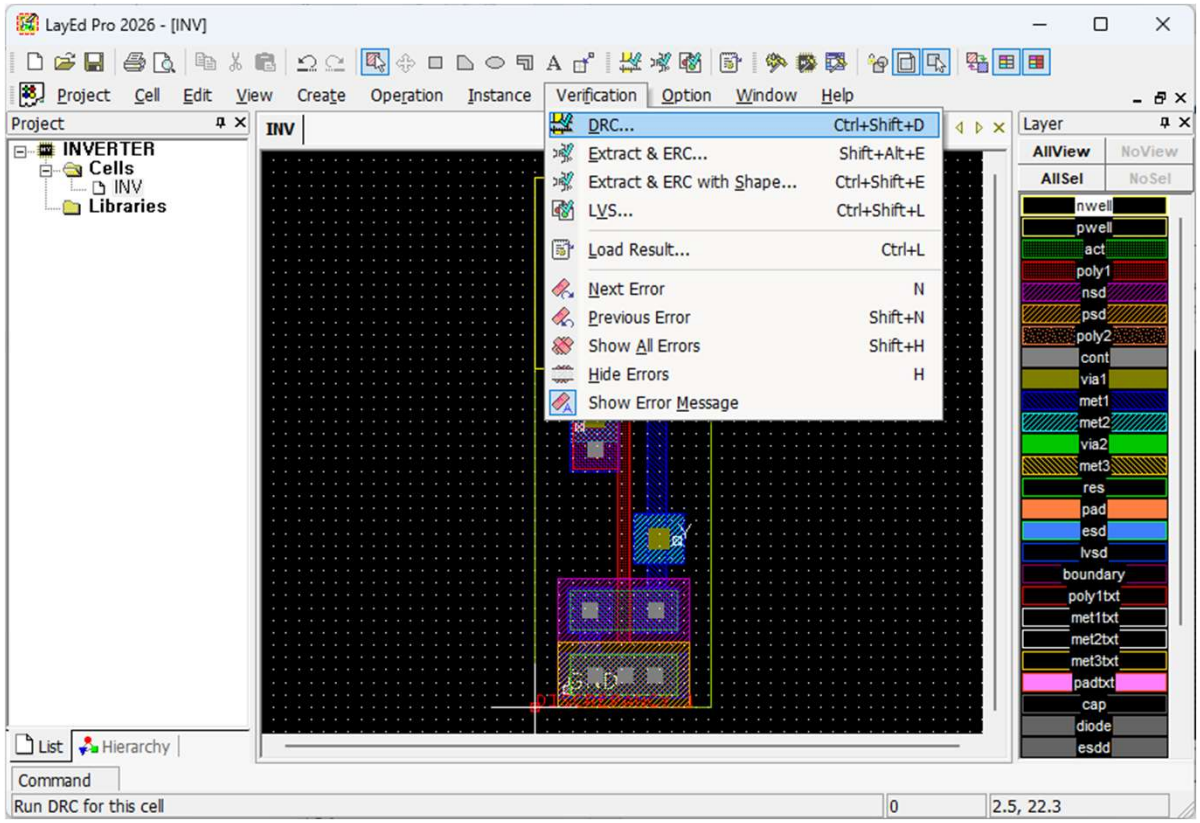


via1/metal2

SELCONN
SELECT & CONNECT

5. Cell design example - Inverter

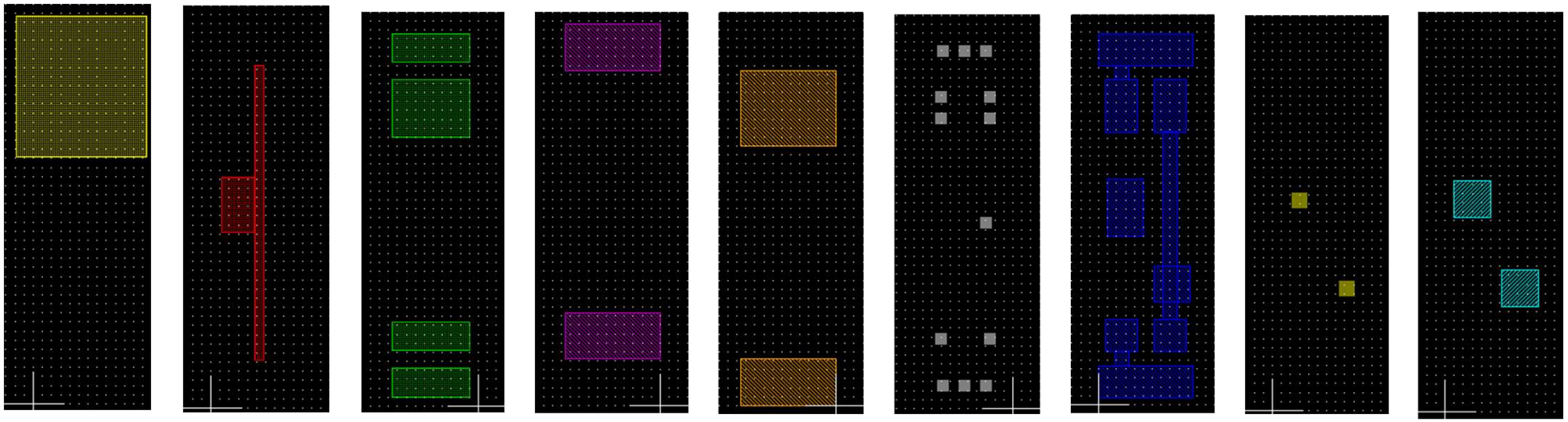
Verification (DRC/ERC/LVS)



SELCONN
SELECT & CONNECT

5. Cell design example - Inverter

Generated Masks

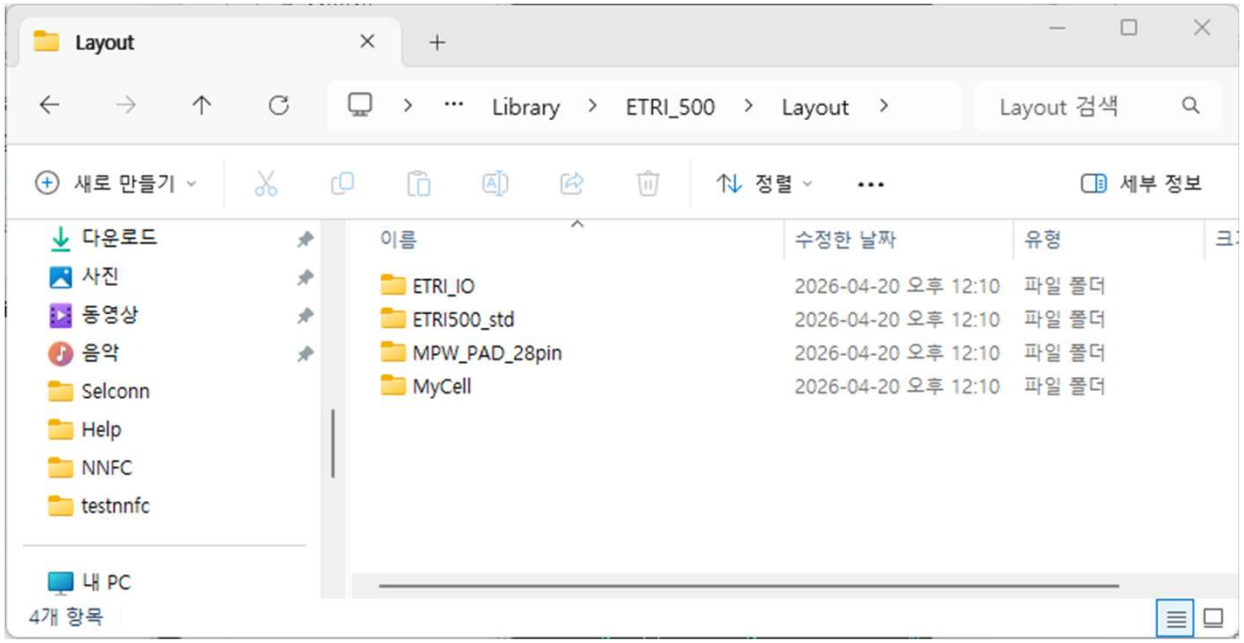


n-well poly1 act nsd psd cont met1 via1 met2

SELCONN
SELECT & CONNECT

6. Design Stopwatch : Circuit (bottom-up)

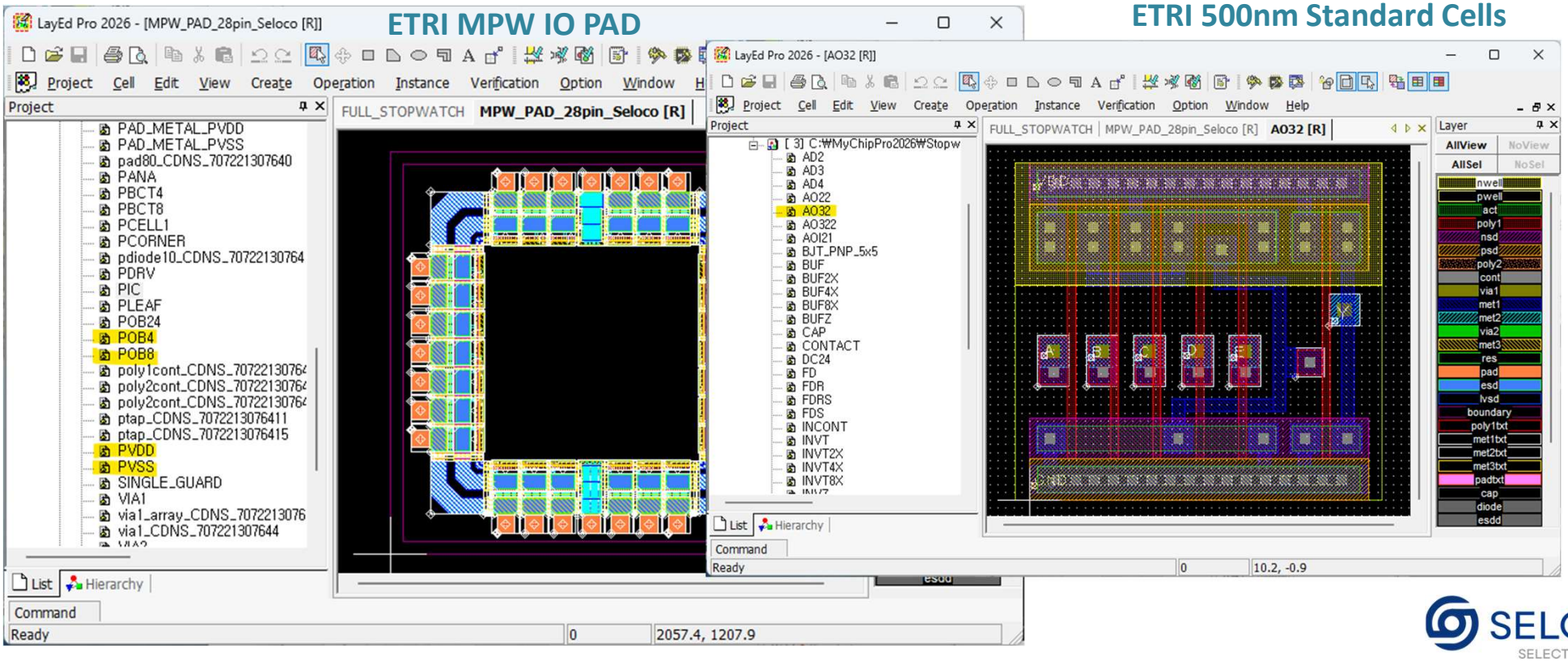
ETRI500 MPW(multi-project on wafer) Platform
ETRI500 Standard Cell library
ETRI500 IO, PAD Library



SELCONN
SELECT & CONNECT

6. Design Stopwatch : Circuit (bottom-up)

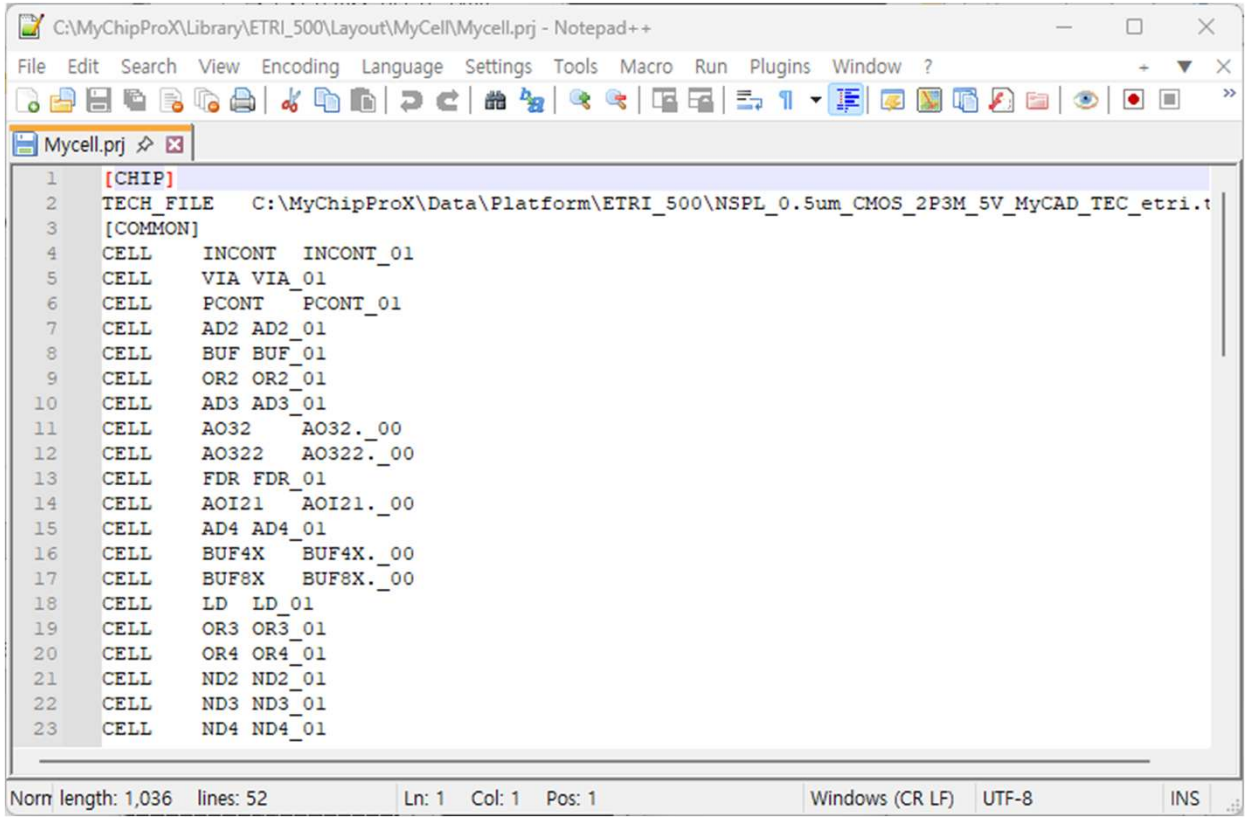
ETRI500 IO, PAD Library – PIC(input pad), POB4(output pad, PVDD, PVSS)
ETRI500 MPW(multi-project on wafer)

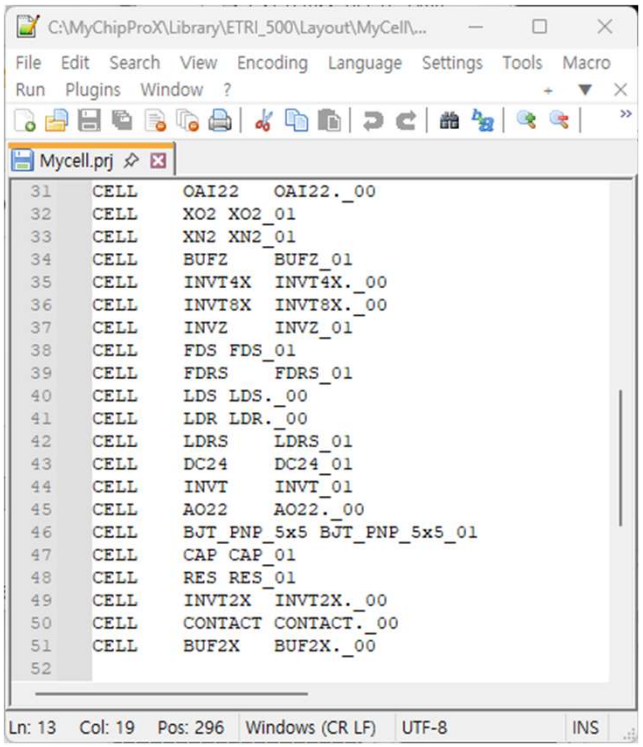


SELCONN
SELECT & CONNECT

6. Design Stopwatch : Circuit (bottom-up)

ETRI500용 Standard Cell – Layout/Circuit, total 48 logic/contact/other cells





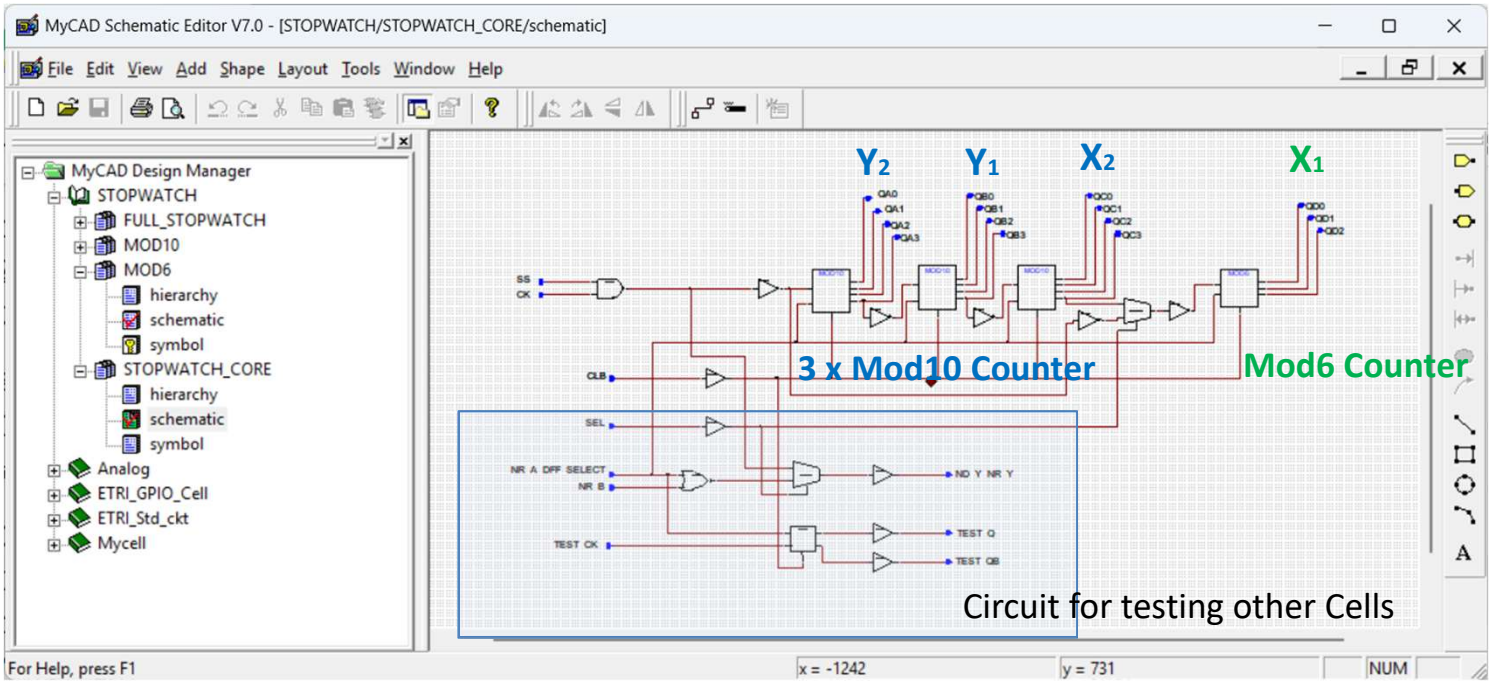
SELCONN
SELECT & CONNECT

6. Design Stopwatch : Circuit (bottom-up)

Modular circuit design on ScheEd.exe

1. 2 digits for SECOND (0~59), 2 digits for CENTI-SECOND (0~99)
2. Start/Pause key, Reset key, Clock(100Hz)
3. 3 BCD counter (0~9 count), 4-pin BCD output
4. 1 mod 6 counter (0~5 count), 3-pin output

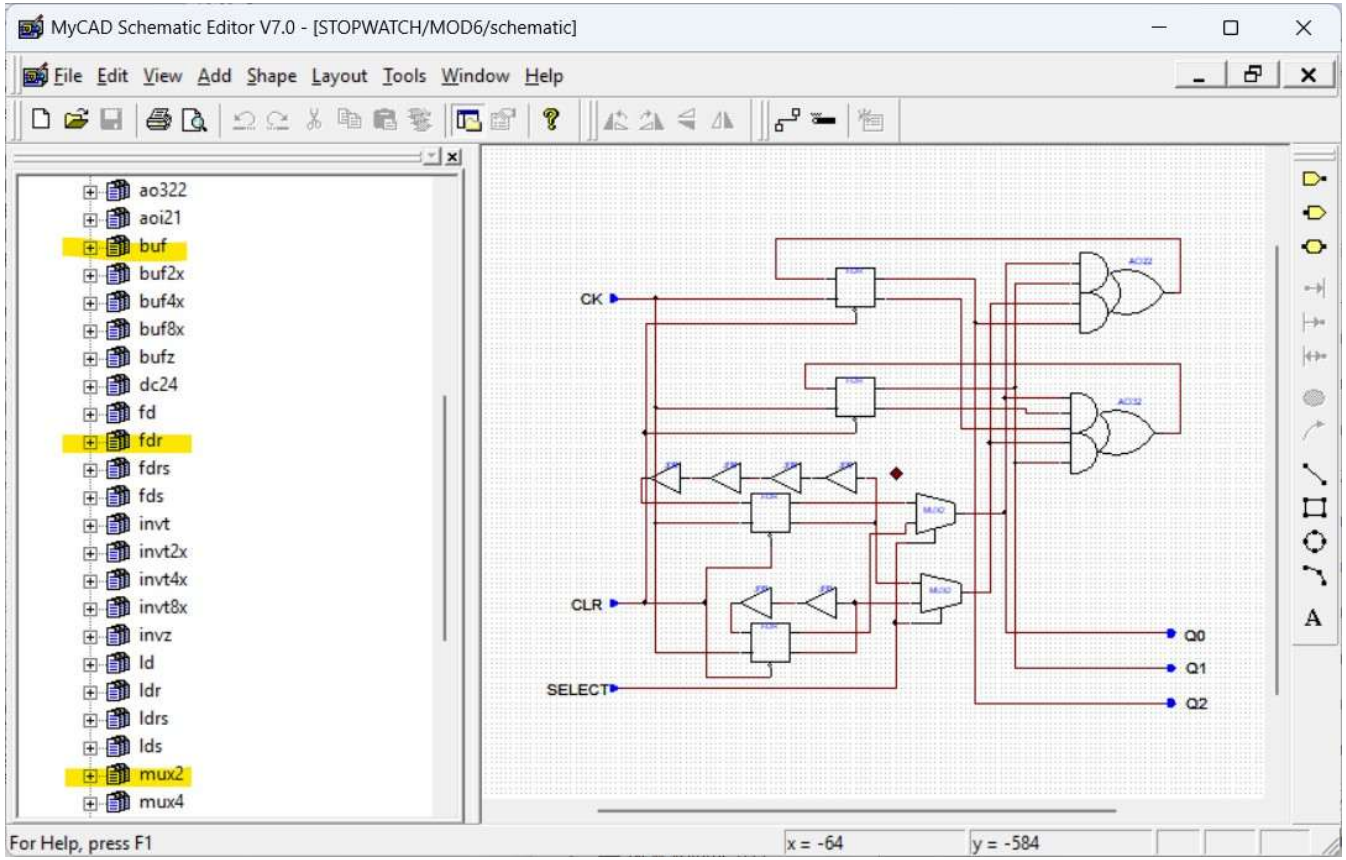
$X_1X_2:Y_1Y_2$



SELCONN
SELECT & CONNECT

6. Design Stopwatch : Circuit (bottom-up)

Mod6 counter



Standard Cell Circuit

4 FDR
flip-flop with Reset
6 BUF
buffer
2 MUX2
2-input mux
1 AO22 cell
OR (2-input AND) (2-input AND)
1 AO32 cell
OR (2-input AND) (3-input AND)

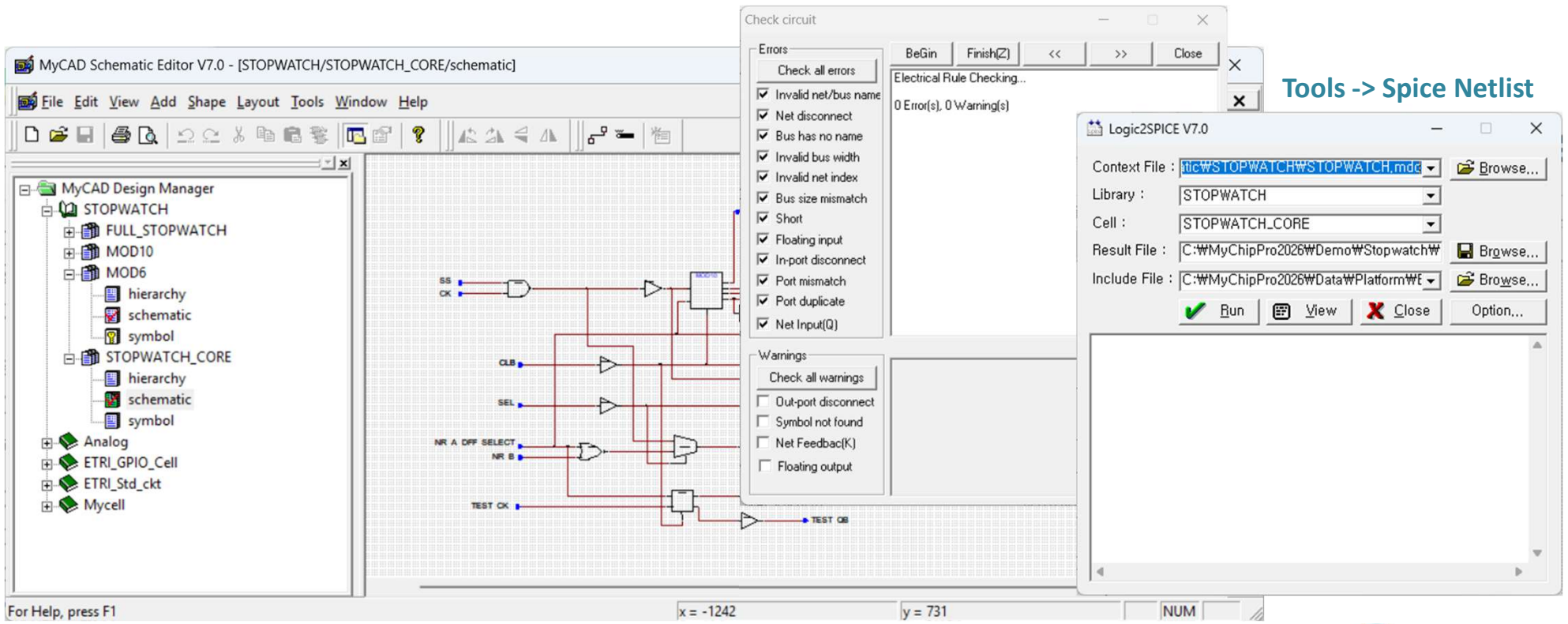
SELCONN
SELECT & CONNECT

6. Design Stopwatch : Circuit (bottom-up)

Check Circuit, Spice Net List Extract

Tools -> Check Circuit

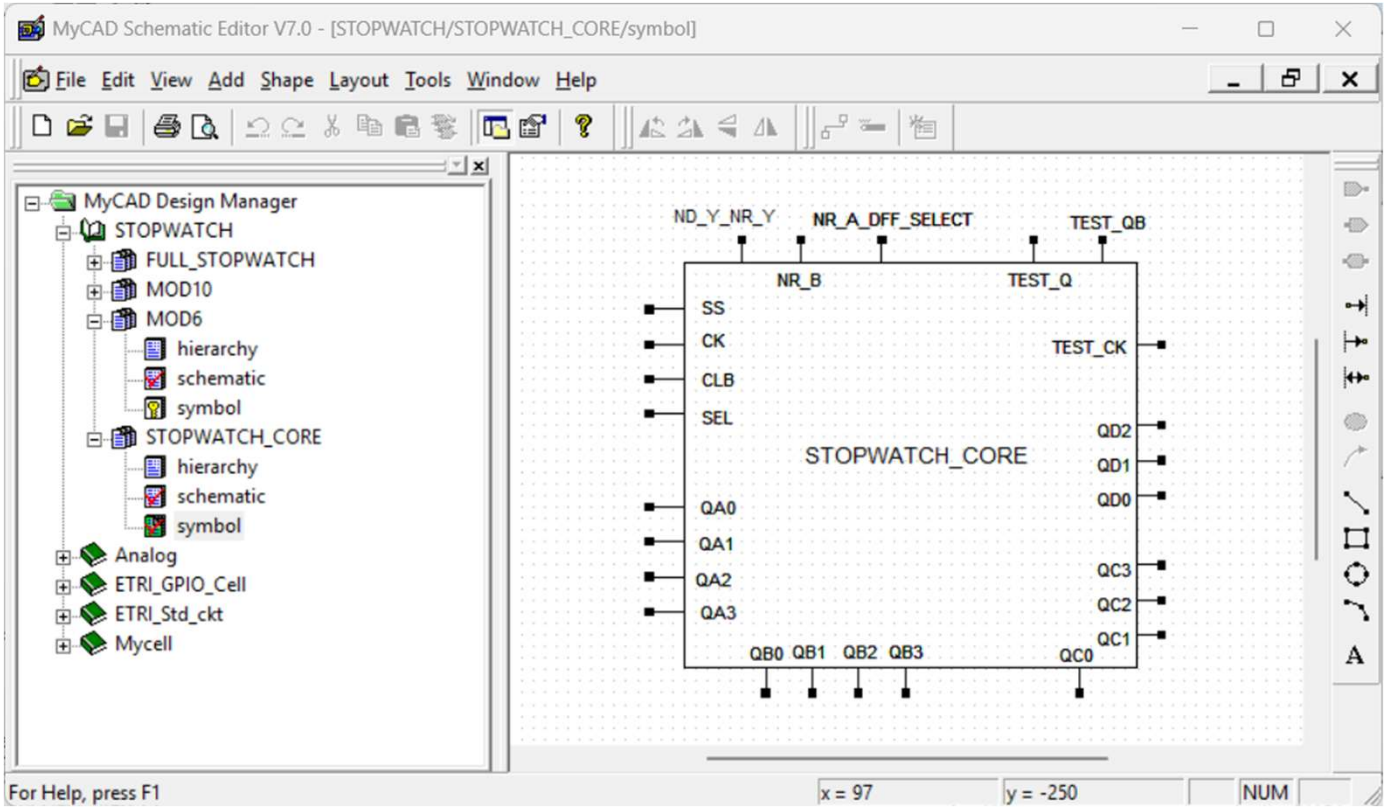
Tools -> Spice Netlist



SELCONN
SELECT & CONNECT

6. Design Stopwatch : Circuit (bottom-up)

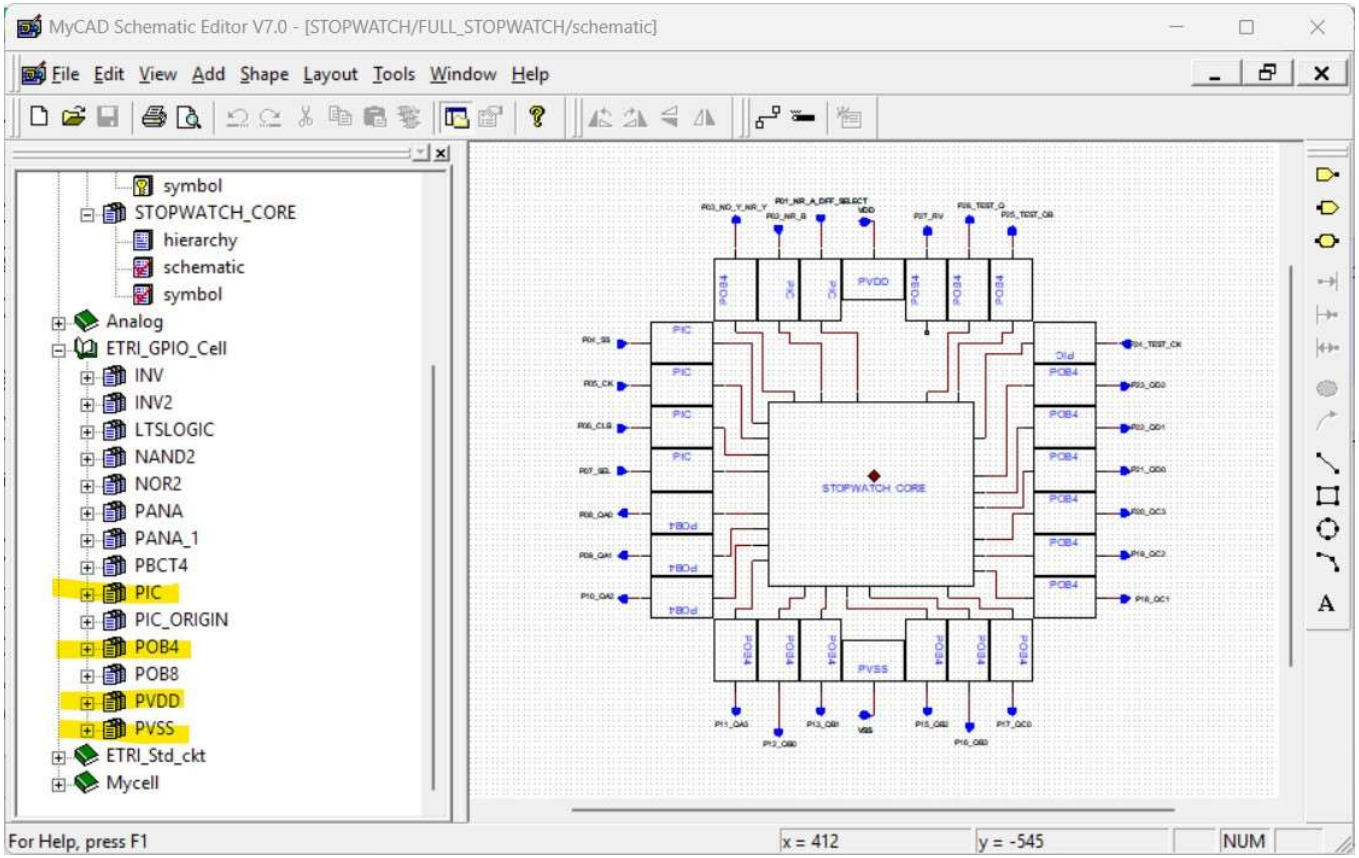
Make Symbol of Stopwatch_core



SELCONN
SELECT & CONNECT

6. Design Stopwatch : Circuit (bottom-up)

Make full_Stopwatch including IO



Connect ETRI IO PAD

PIC – input PAD
POB4 – output PAD
PVDD – VDD PAD
PVSS – GND PAD

Extract Spice Netlist

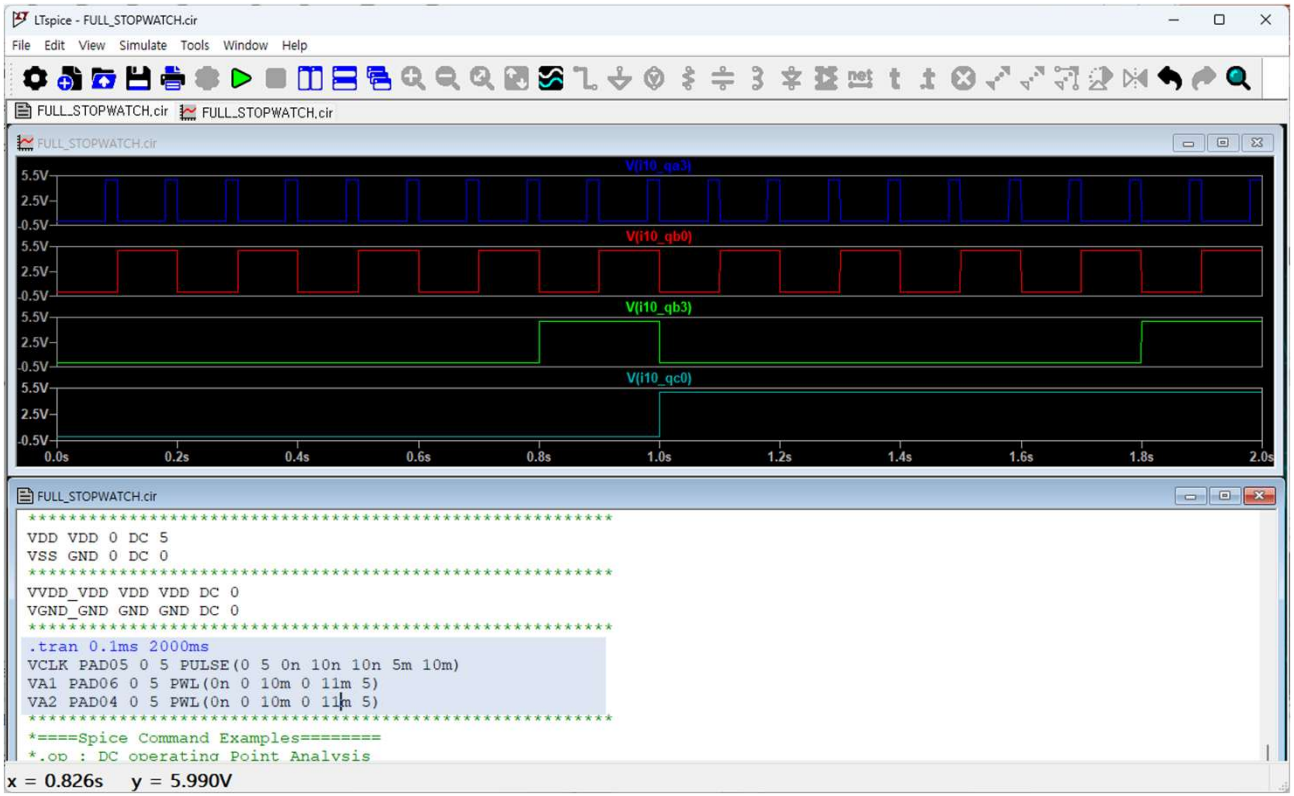
(it will be used for comparing with final layout)

SELCONN
SELECT & CONNECT

6. Design Stopwatch : Circuit (bottom-up)

Spice Simulation using extracted spice netlist

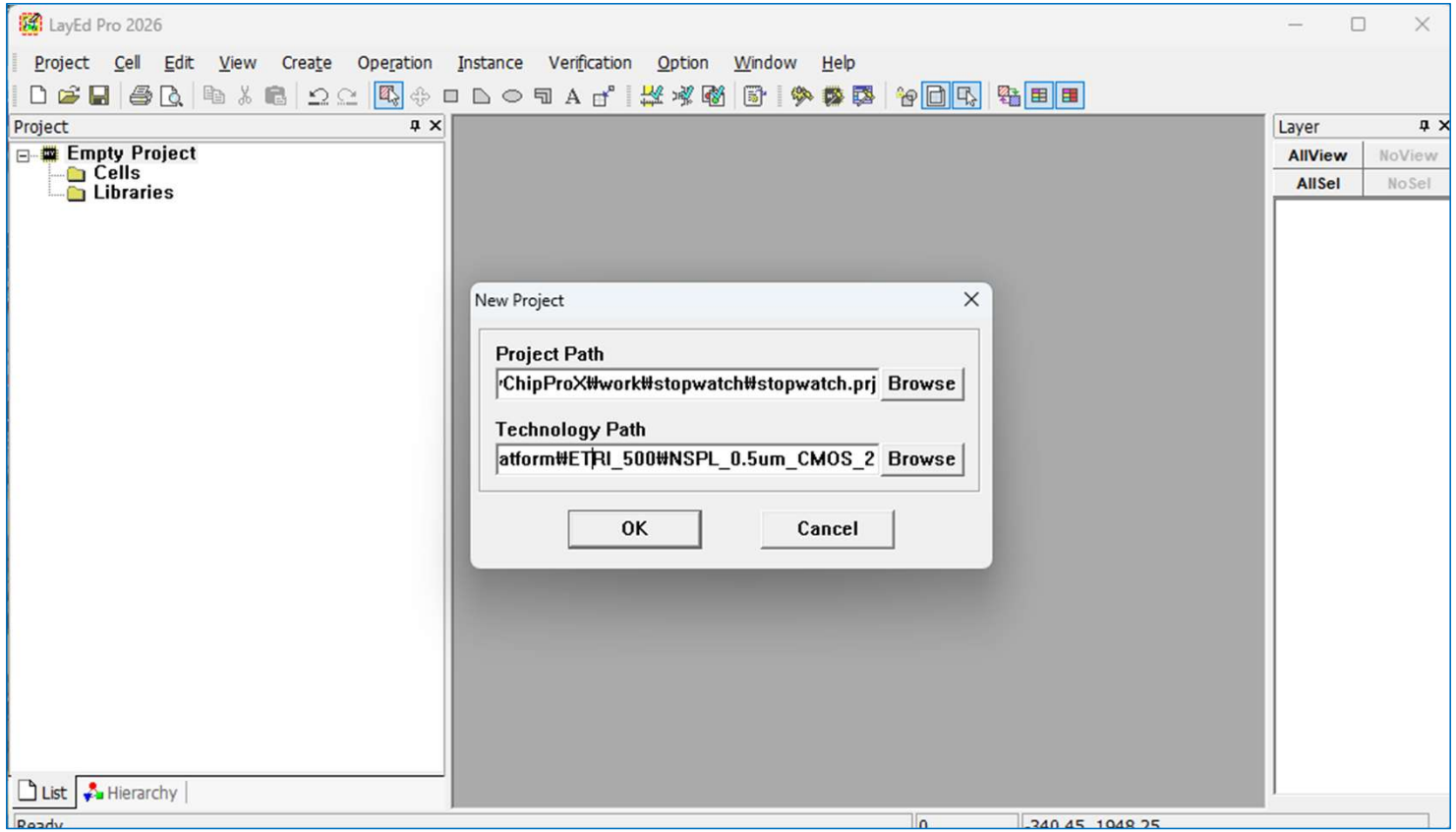
- Simulation using netlist from Schematic (LTspice)
- SPICE Simulation
  - PAD05 -> CK
  - PAD06-> CLB
  - PAD11 -> QA3
  - PAD12 -> QB0
  - PAD15 -> QB3
  - PAD16 -> QC0
  - .99s -> 1s



SELCONN
SELECT & CONNECT

6. Design Stopwatch : Layout (bottom-up)

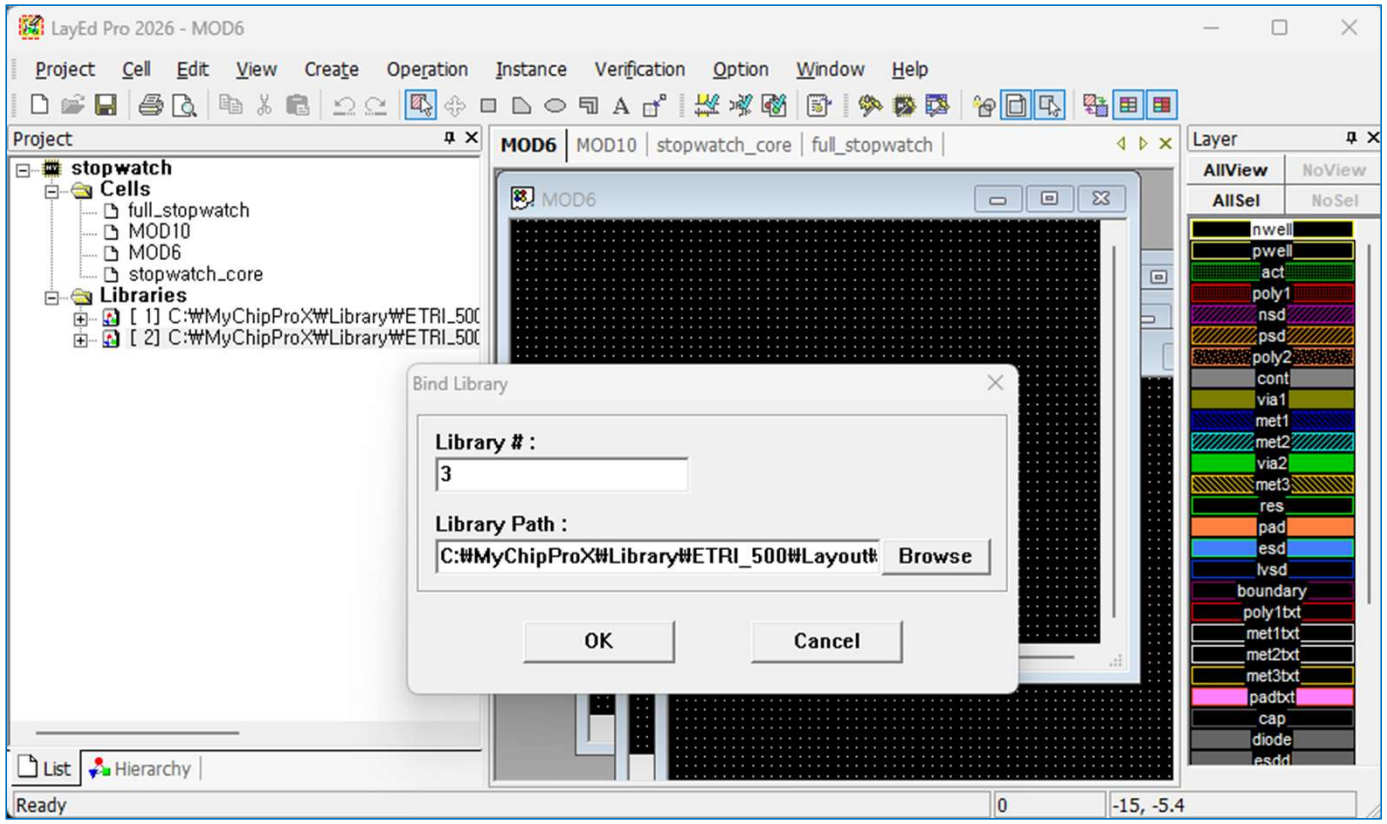
Stopwatch project generation using ETRI 500 platform – LayEdPro.exe



SELCONN
SELECT & CONNECT

6. Design Stopwatch : Layout (bottom-up)

Create Cells and Binding Libraries



Project -> Bind Library…

Library\ETRI_500\Layout
- EYTRI_IO
- MyCell
- MPW_PAD_28pin_Seloco

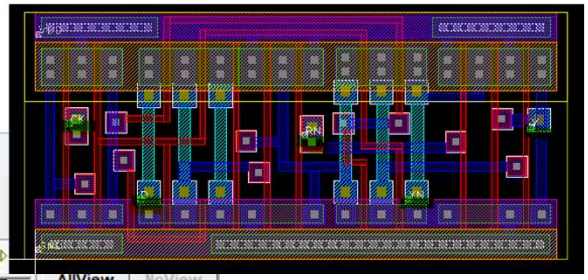
SELCONN
SELECT & CONNECT

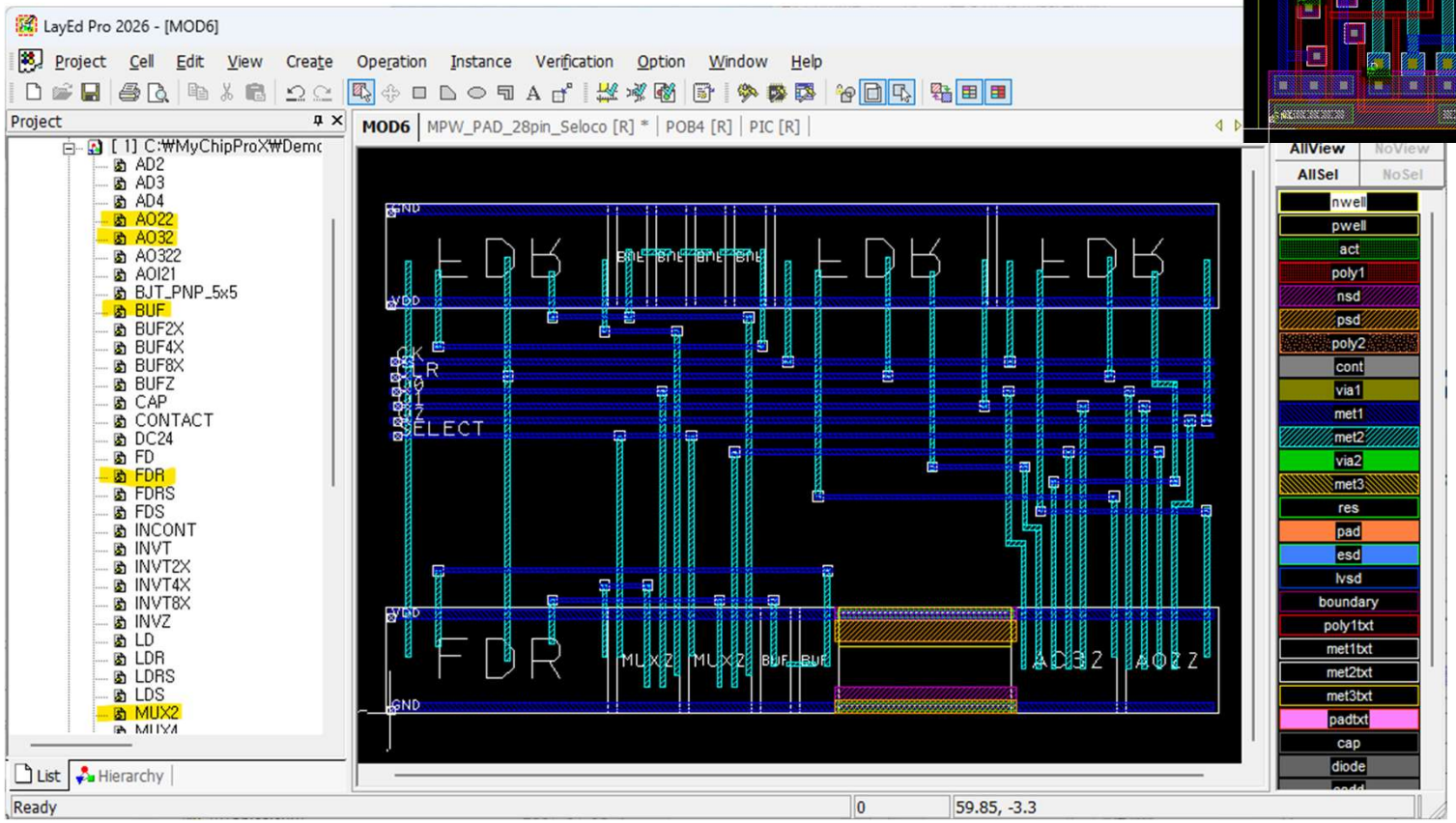
6. Design Stopwatch : Layout (bottom-up)

Design mod6 Layout on LayEdPro.exe

Place Cells and connect each cell based on Mod6 counter Circuit

FDR cell





4 FDR cells
flip-flop with Reset
6 BUF cells
buffer
2 MUX2 cells
2-input mux
1 AO22 cell
OR (2-input AND) (2-input AND)
1 AO32 cell
OR (2-input AND) (3-input AND)

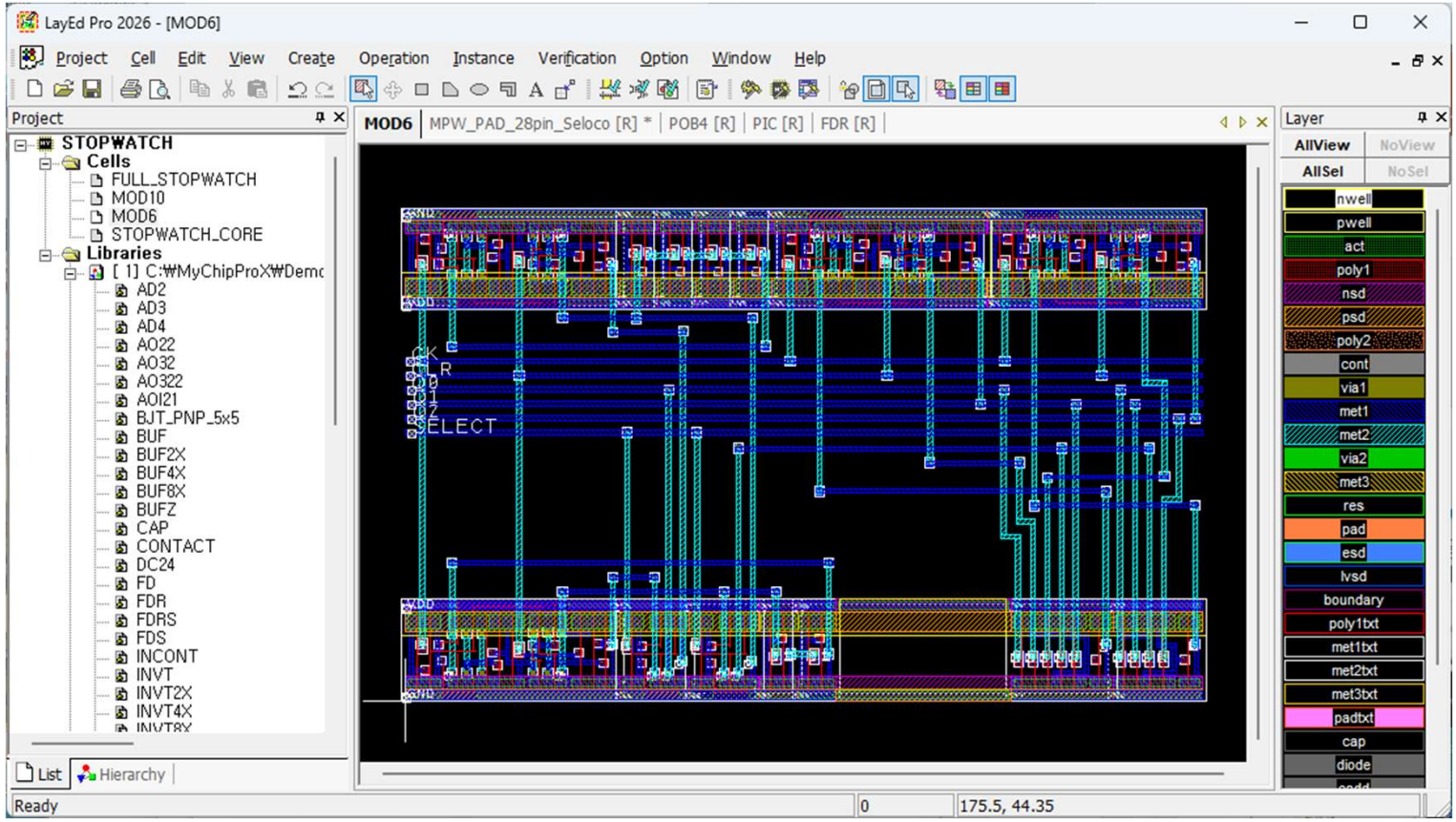
Connect each cell using metal/via
after placement

Run DRC Frequently
During Layout Design

SELCONN
SELECT & CONNECT

6. Design Stopwatch : Layout (bottom-up)

Designed Mod 6 layout - Flattened View

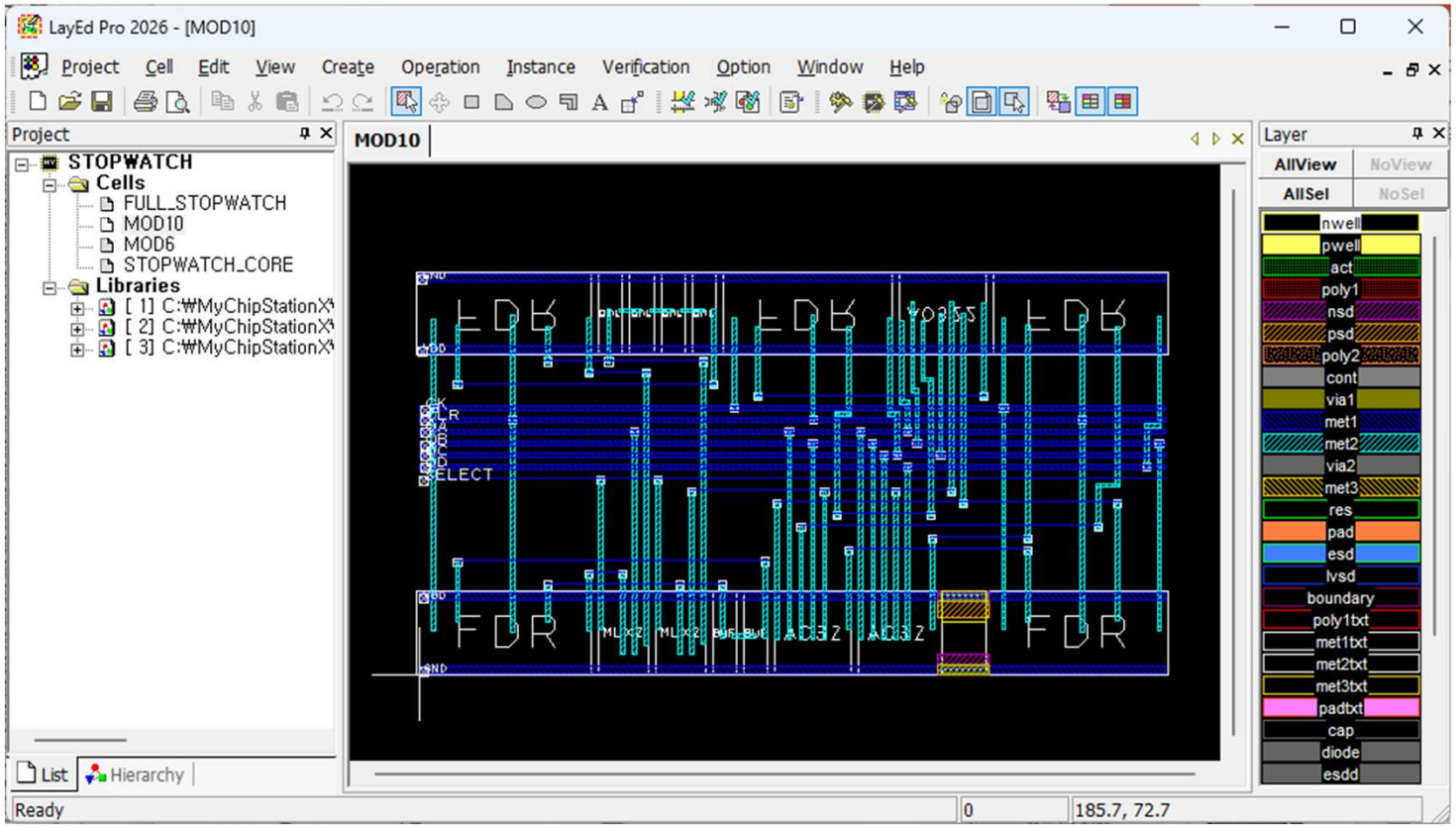


SELCONN
SELECT & CONNECT

6. Design Stopwatch : Layout (bottom-up)

Design mod 10 Layout on LayEdPro.exe

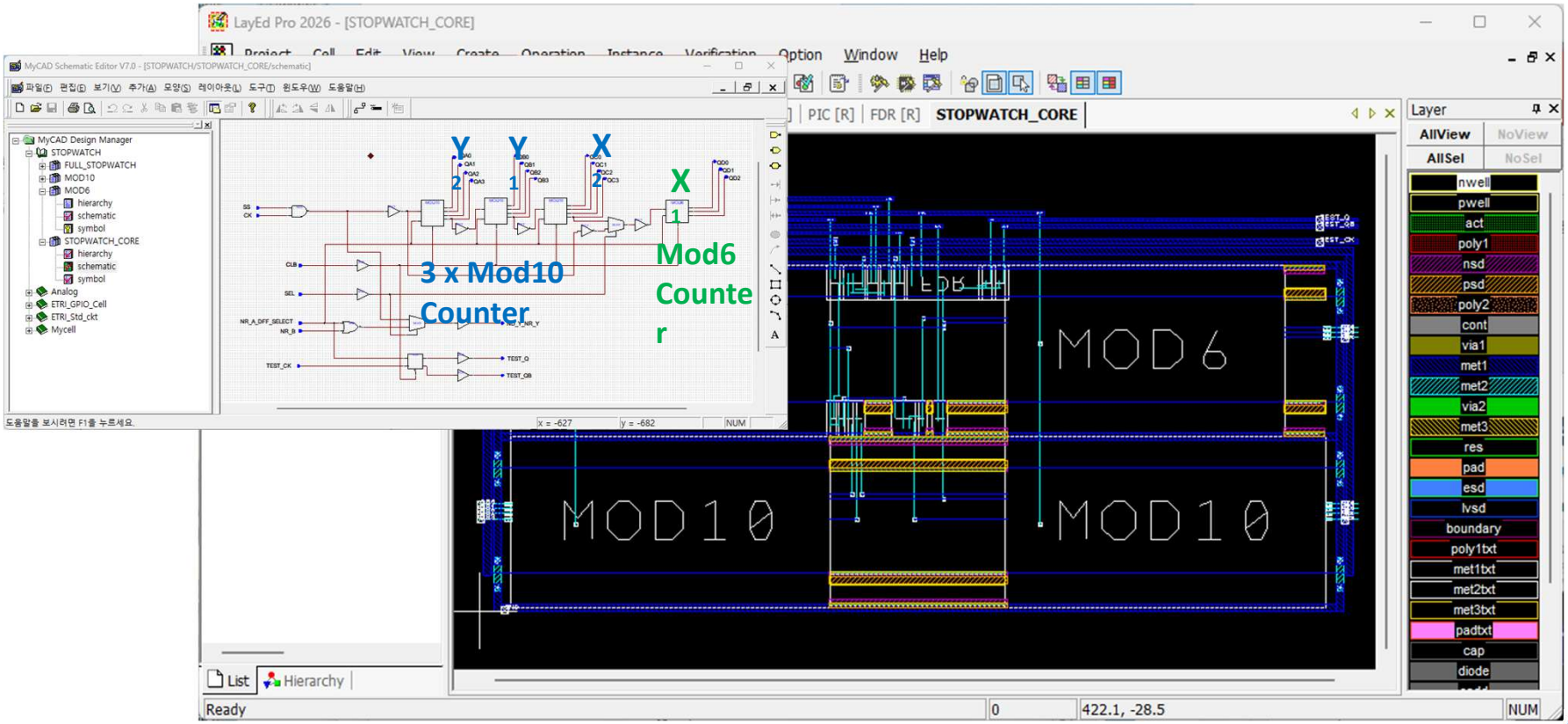
Place Cells and connect each cell based on Mod 10 BCD counter Circuit



SELCONN
SELECT & CONNECT

6. Design Stopwatch : Layout (bottom-up)

Design Stopwatch core using mod10 and mod6 based on stopwatch_core circuit

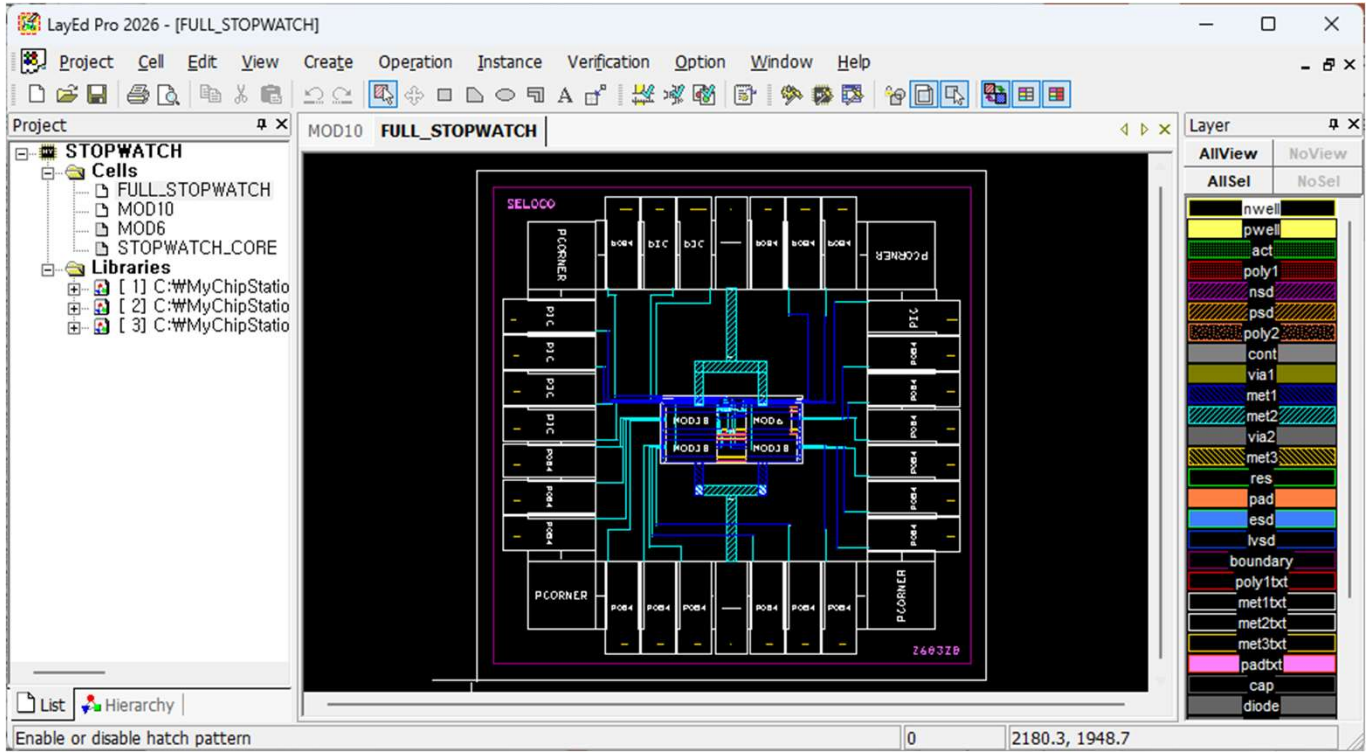


SELCONN
SELECT & CONNECT

6. Design Stopwatch : Layout (bottom-up)

Stopwatch Completion – Connecting the Stopwatch Core to the I/O Pads for the ETRI MPW

- Create a new cell named **Full_stopwatch**. Load the **28-pin pad frame** and **Stopwatch_core** from the library.
- Connect the I/Os of the **Stopwatch_core** to the I/Os of the **28-pin MPW pad frame**
- Replace each I/O pad with an **input pad** or **output pad** as needed.

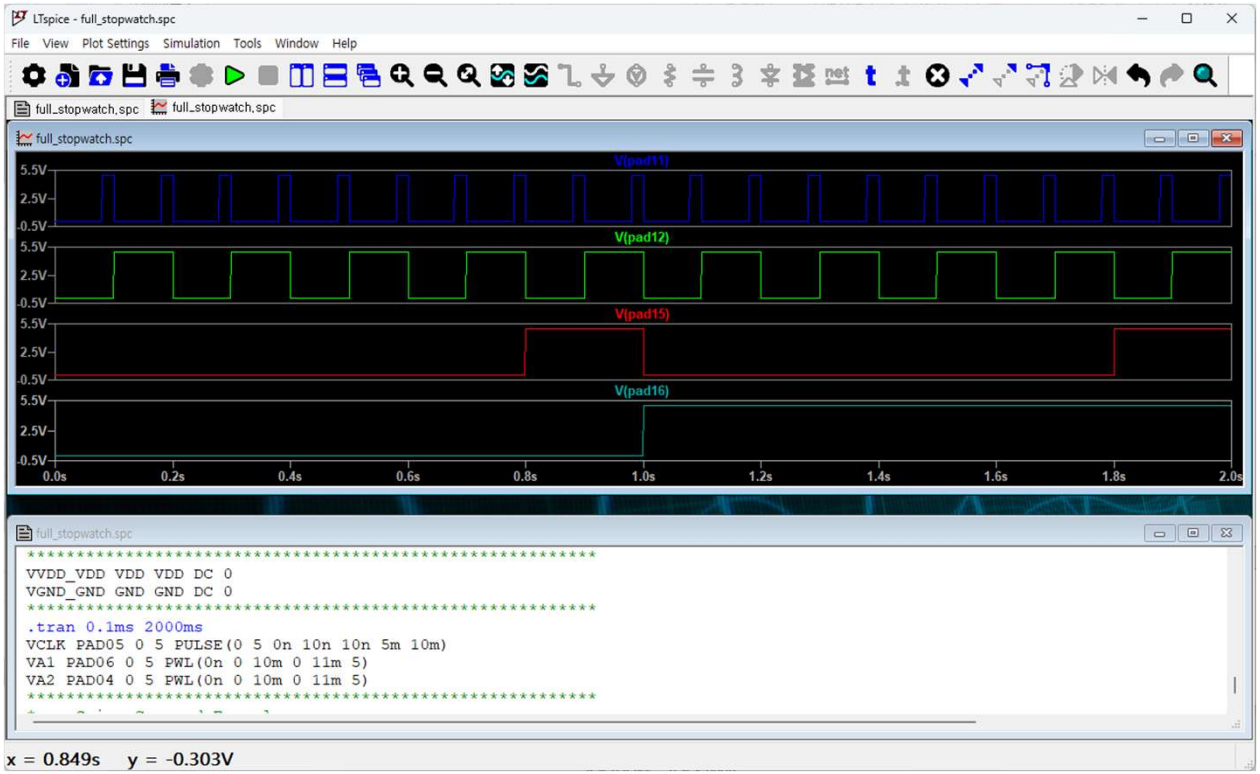


SELCONN
SELECT & CONNECT

6. Design Stopwatch : Layout (bottom-up)

Check the result of Layout Spice Simulation (EXTRACT.1 file under design folder, extracted by MyNetPro)

- Simulation using netlist extracted from layout
- Spice Simulation
  (LayEdPro->MyNetPro)
  - PAD05 -> CK
  - PAD06-> CLB
  - PAD11 -> QA3
  - PAD12 -> QB0
  - PAD15 -> QB3
  - PAD16 -> QC0
  - .99s -> 1s



SELCONN
SELECT & CONNECT

6. Design Stopwatch : Layout (bottom-up)

Manual (bottom-up) Layout Design Flow Summary

1.Select the Target Fabrication Platform : Choose the semiconductor process (platform) for chip fabrication.

2.Verify the Available Standard Cell Library : Confirm the available standard cells (layout and circuit).

3.Design and Verify the Chip Functionality

1. Implement the chip using standard cells (**modular design**).
2. Verify the circuit schematic.

4.Create a New Layout Project : Create a project in the Layout Editor using the selected platform.

5.Create Blank Cells and Bind the Library

1. Create a blank cell for each module.
2. Bind the platform-specific library.

6.Design the Layout of Each Module

1. Place the required standard cells.
2. Connect them using metal layers and vias.

7.Perform DRC During Layout Design : Run DRC frequently to detect design rule violations.

8.Design the logic core using designed modules

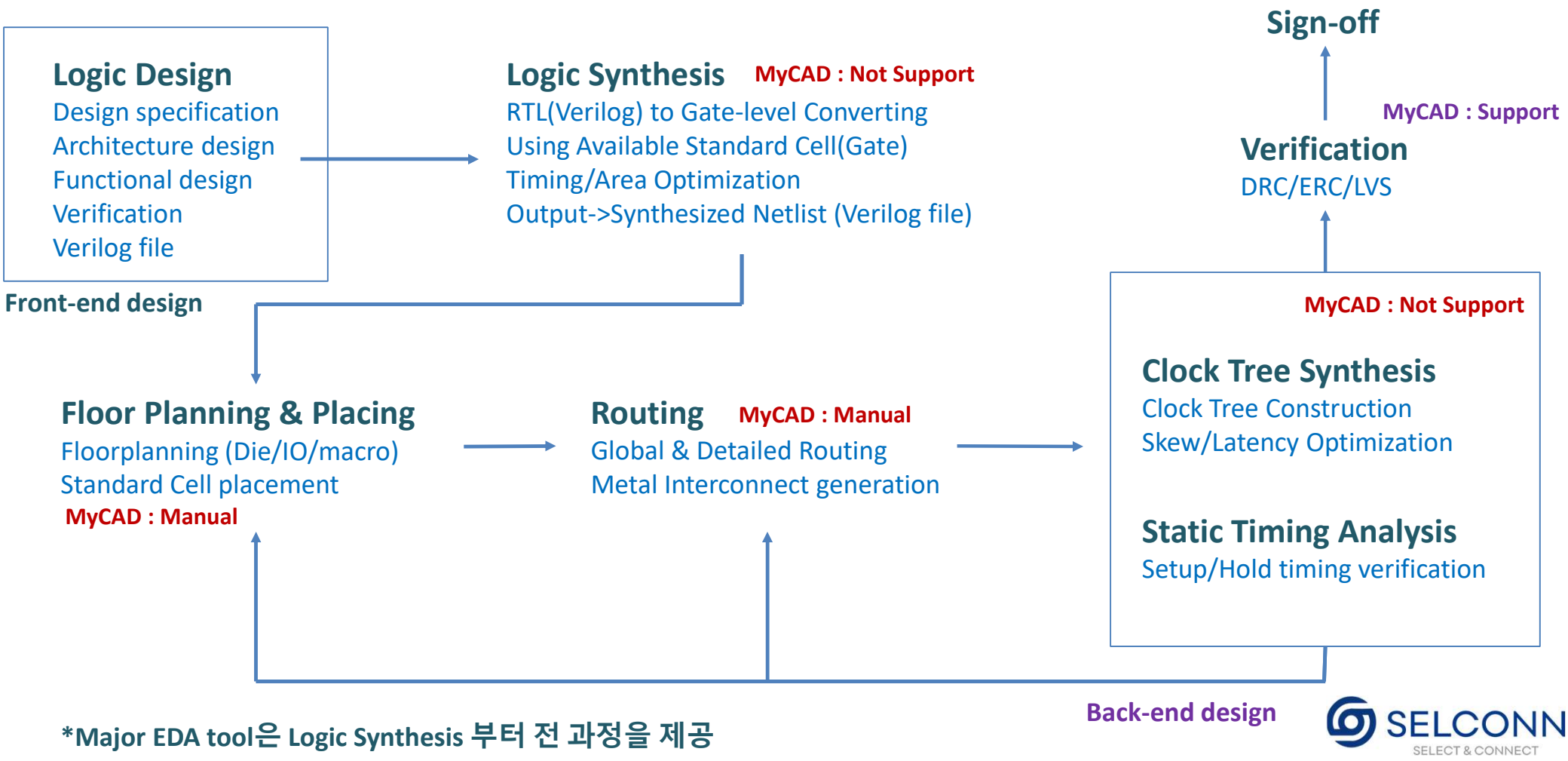
9.Verify the Logic Core : Perform **DRC, ERC, and LVS** after completing the logic core.

10.Integrate the I/O Pads : Connect the **ETRI MPW I/O pad frame** to the **Stopwatch core**.

11.Final Verification : Perform the final **DRC, ERC, and LVS** before tape-out.

SELCONN
SELECT & CONNECT

7. Top-down Chip Design Process



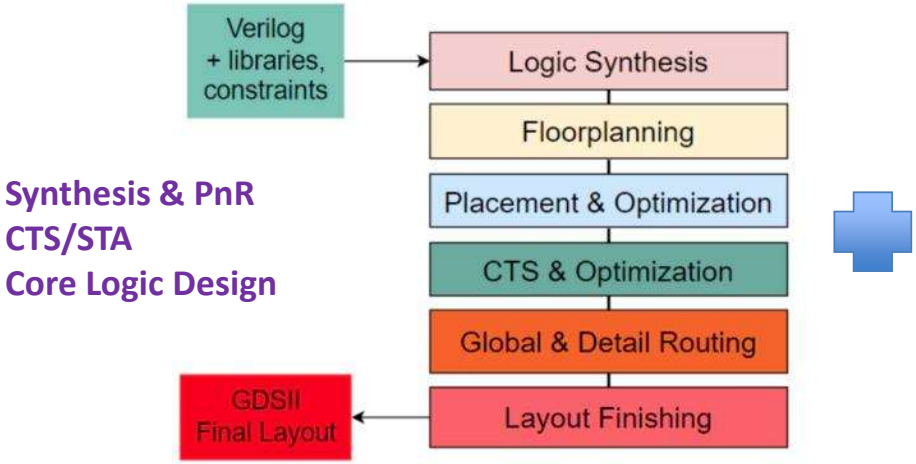
*Major EDA tool은 Logic Synthesis 부터 전 과정을 제공

SELCONN
SELECT & CONNECT

7. Top-down Chip Design Process – OpenROAD & MyChipStationX

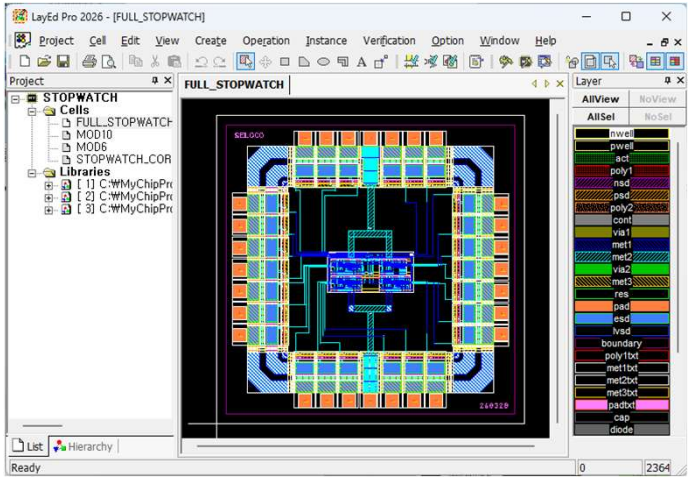
OpenROAD + MyCAD: Best Combination

- **OpenROAD**: Open-source RTL-to-GDS ASIC design automation toolchain
  - **Focus**: Physical design / backend design
  - **Limitations**: Linux-based, script-driven, limited GUI layout editing
- **MyChipStationX**: Windows-based layout editing, verification, and visualization
- **Integration**: Seamless connection between Linux-based OpenROAD and Windows-based MyChipStationX
- **Result**: Automated digital design flow with powerful layout editing capability



Synthesis & PnR
CTS/STA
Core Logic Design

OpenROAD

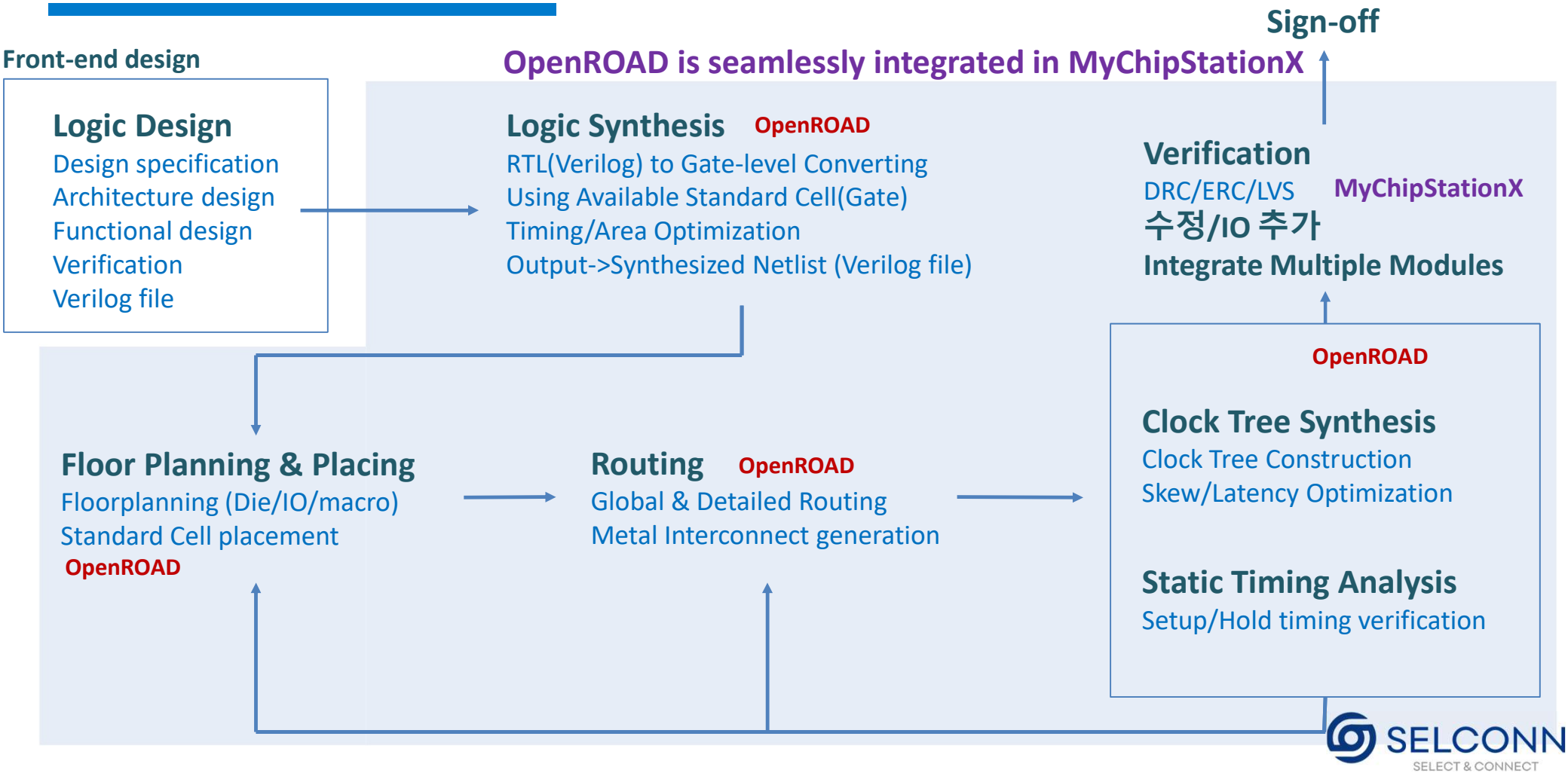


Layout Editing
Verification
Add IO PAD
Mixed Signal Design

MyChipStationX

SELCONN
SELECT & CONNECT

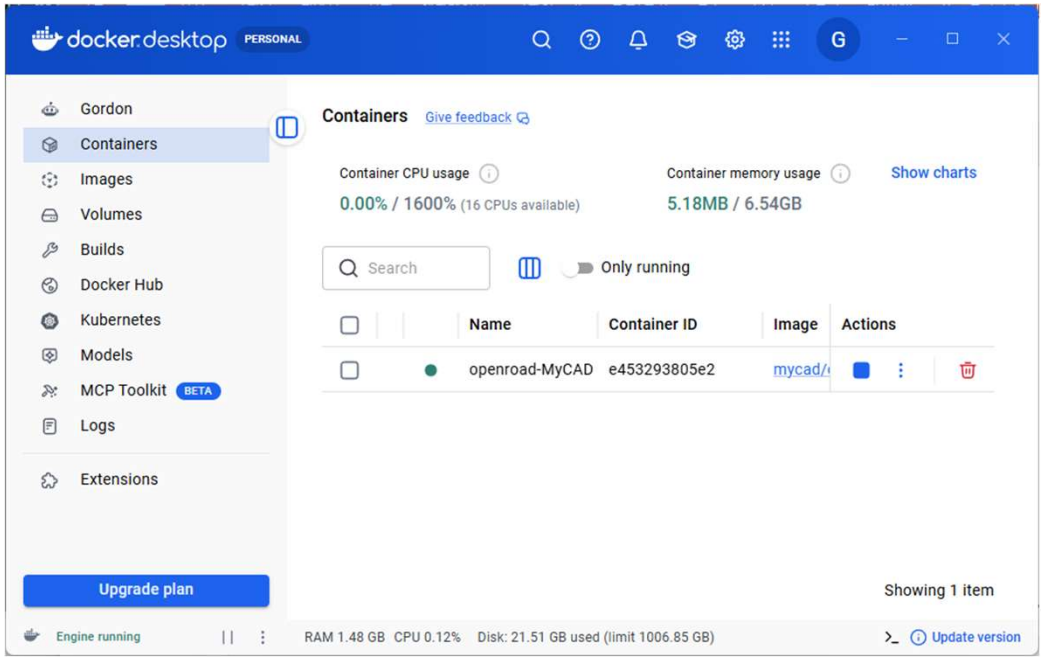
7. Top-down Chip Design Process – OpenROAD & MyChipStationX



SELCONN
SELECT & CONNECT

7. Top-down Chip Design Process – Setup OpenROAD Environment

1. Install WSL (Ubuntu) from Microsoft Store
2. Install Docket Desktop from Microsoft Store
   (Please check Hyper-V is enabled on BIOS)
3. Make an account for Docker and log-in
4. Run Docker Desktop on Windows
5. Make a Docker container as below to share
   C:\MyChipStationX\openroad and /flow/MyCAD
   on OpenROAD



on Windows Power Shell

PS C:\Users\User> docker run -it --name openroad-MyCAD -v C:\MyChipStationX\openroad:/OpenROAD-flow-scripts/flow/MyCAD mycad/openroad:v1 bash

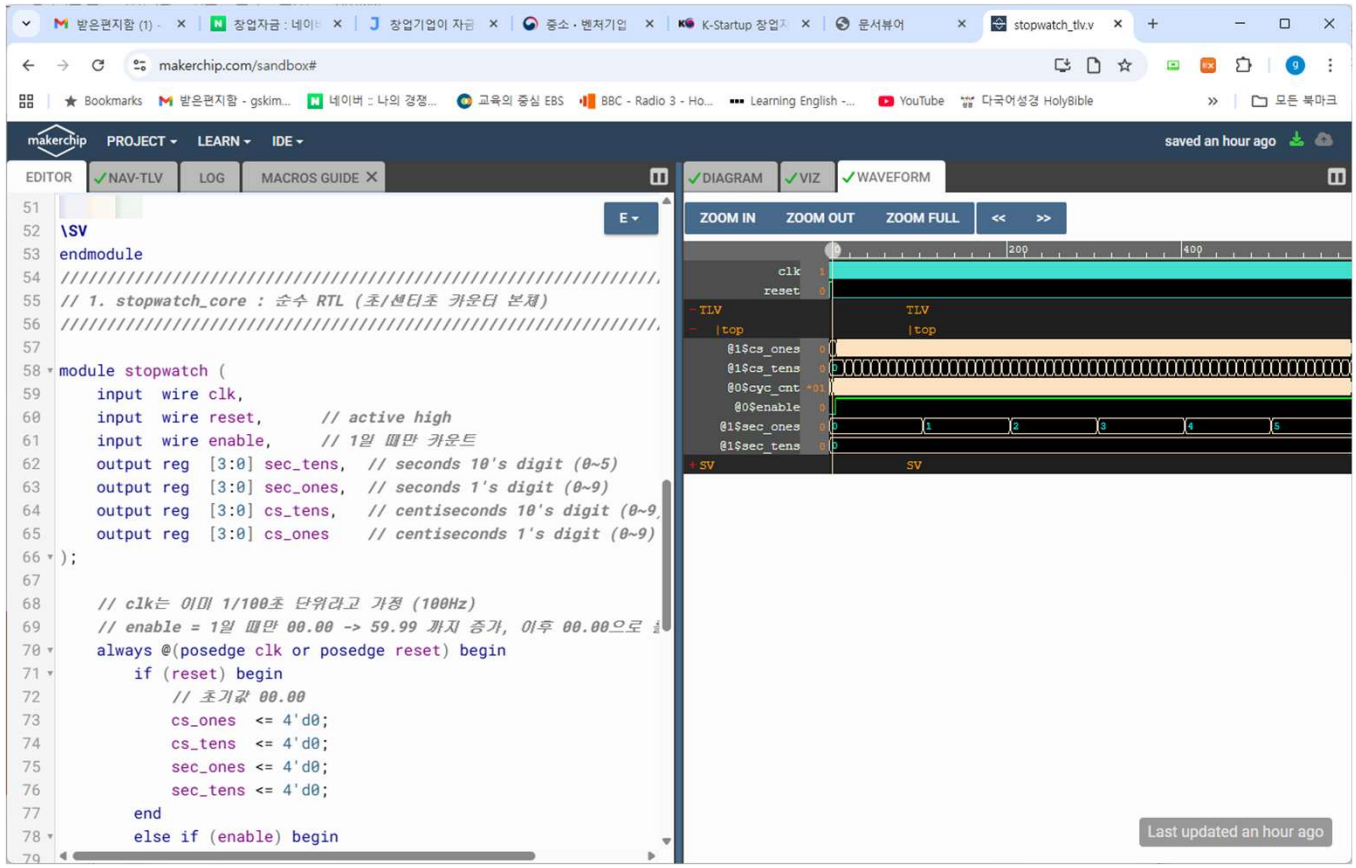
Now You Are ready to use MyOpenROAD.exe to use OpenROAD for synthesis and PnR

You need to Run Docker Desktop and openroad-MyCAD must be active

SELCONN
SELECT & CONNECT

8. Stopwatch Design (Front-end) - Stopwatch logic design(verilog)

Verilog design and Simulation Example(Makerchip solution & ChatGPT)



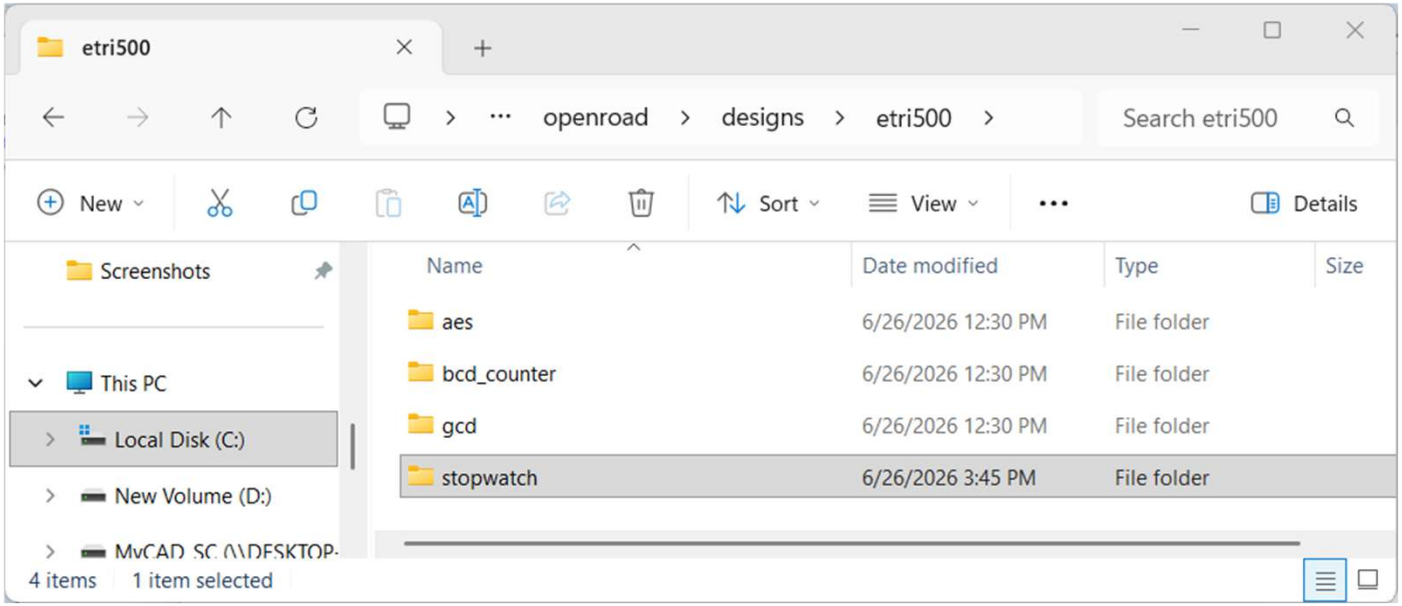
ChatGPT Input and Makerchip Simulation

- Enter the design requirement into **ChatGPT**:
  - Create a stopwatch in Verilog with:
    - **100 Hz clock input**
    - **Enable signal** for start/pause control
    - **Reset signal**
    - **BCD outputs** for:
      - Two-digit centiseconds
      - Two-digit seconds
- Ask ChatGPT to generate a **Verilog-TLV version** by adding a **TLV header** to the Verilog code.
- Load the generated **verilog.tlv** file on www.makerchip.com.
- Run the simulation on the **Makerchip** website and verify the stopwatch operation.

SELCONN
SELECT & CONNECT

8. Stopwatch Design (Top-down) – Configuring Design Source file

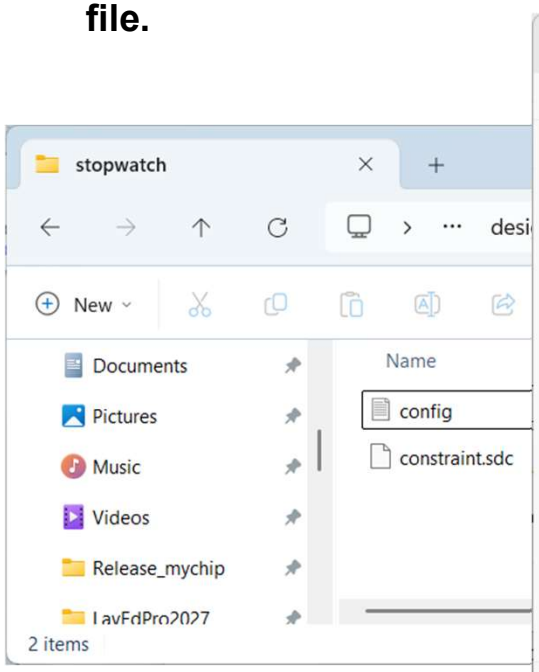
1. **Make design source folder(stopwatch) under C:\MyChipStationX\openroad\designs\src**
2. **Copy verilog source file(stopwatch.v) into this new folder.**



SELCONN
SELECT & CONNECT

8. Stopwatch Design (Top-down) – Configuring Design Source file

1. Create ne folder(stopwatch) under C:\MyChipStationX\openroad\designs\etri500 (you may copy one of existing folder and rename it).
2. Create or edit config.mk file as below. And change the design name to stopwatch in constraint.sdc file.



config.mk

File Edit View

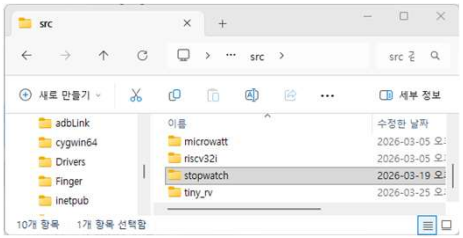
```
#DESIGN_NICKNAME : folder name where the source verilog file and design config.mk is located
export DESIGN_NICKNAME = stopwatch
#PLATFORM : design platform, etri500 or sky130hd
export PLATFORM    = etri500
#DESIGN NAME : Name of starting module
export DESIGN_NAME = stopwatch

export VERILOG_FILES = $(DESIGN_HOME)/src/$(DESIGN_NICKNAME)/stopwatch.v
#if there are more than one verilog files
#export VERILOG_FILES = $(DESIGN_HOME)/src/$(DESIGN_NICKNAME)/*.v
export VERILOG_FILES = $(DESIGN_HOME)/src/$(DESIGN_NICKNAME)/stopwatch.v
export SDC_FILE      = $(DESIGN_HOME)/$(PLATFORM)/$(DESIGN_NICKNAME)/constraint.sdc

export CORE_UTILIZATION = 30
export TNS_END_PERCENT = 100

#Allow via on PIN of each cell
export DETAILED_ROUTE_ARGS += -via_in_pin_bottom_layer met1 -via_in_pin_top_layer met3
```

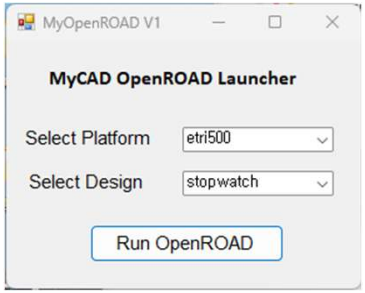
Ln 18, Col 87 | 793 characters | Plain text | 100% | Unix (LF) | UTF-8

SELCONN
SELECT & CONNECT

8. Stopwatch Design (Top-down) – Design flow

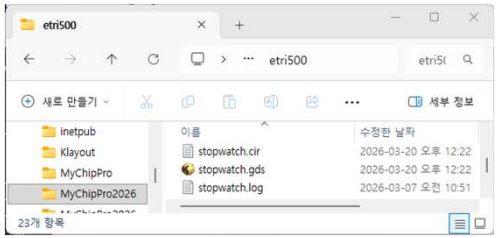
1. Design (Verilog) & Scripts (On Windows)

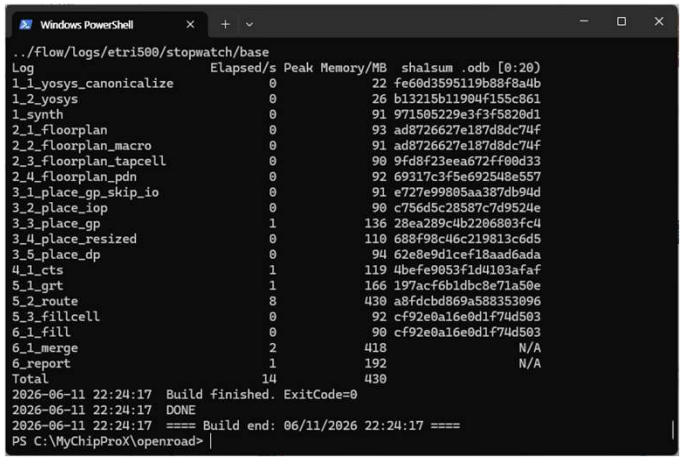




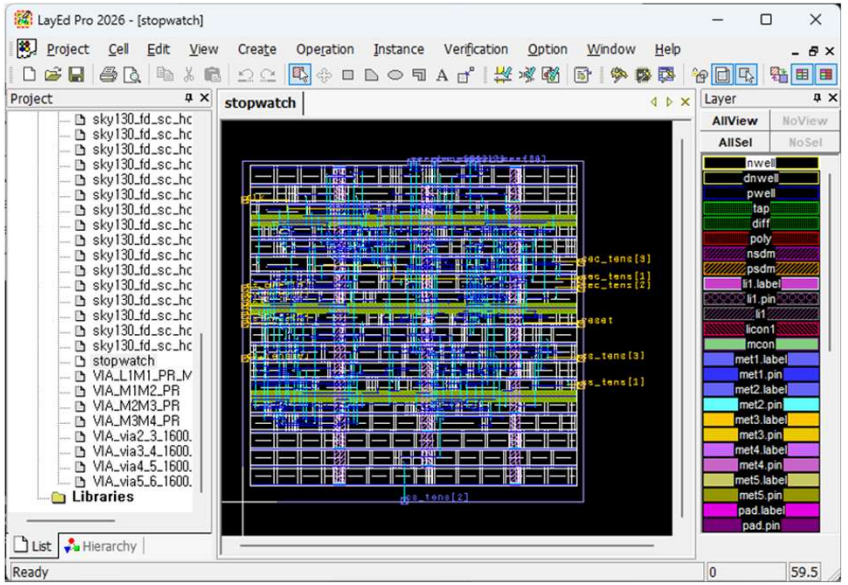
2. Execute OpenROAD

4. Final results(GDSII, netlist..) on Windows





3. OepnROAD Result (Synthesis & PnR)

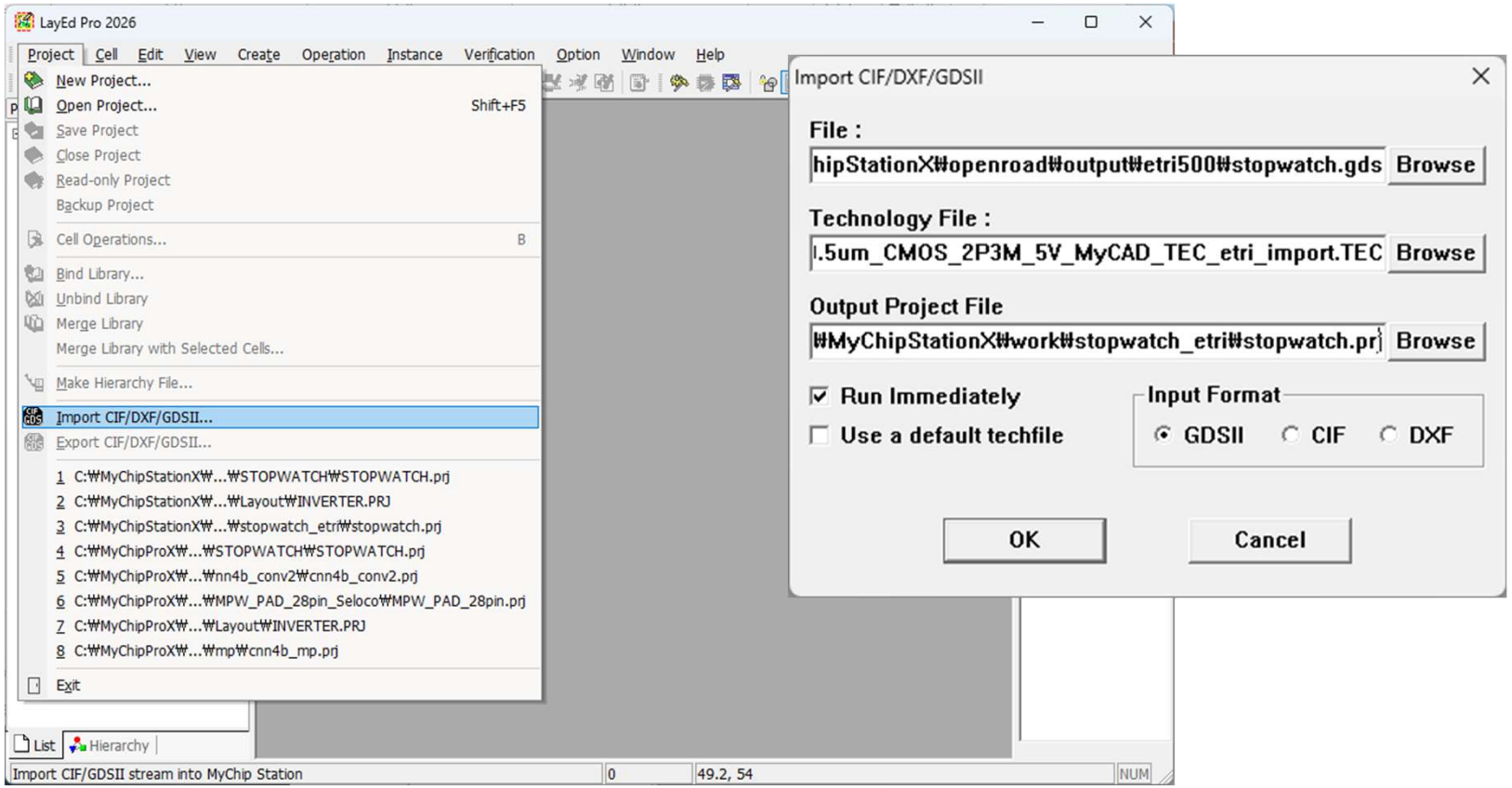


5.Editing & Verification on MyChipStationX

SELCONN
SELECT & CONNECT

8. Stopwatch Design (Top-down) – Import Result into MyChipStationX

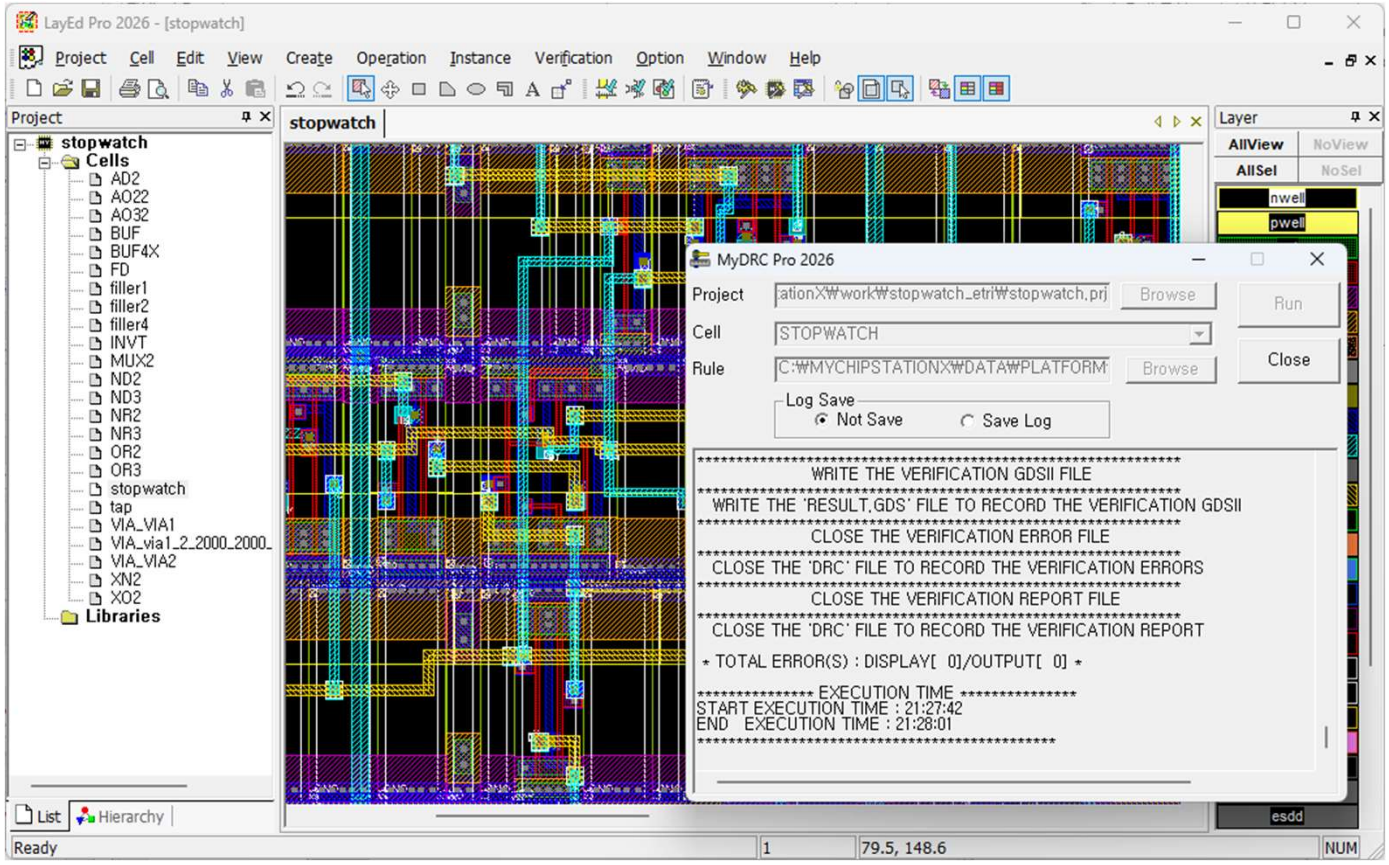
Import result of OpenROAD(at openroad\output\etri500\) into MyChipStationX



SELCONN
SELECT & CONNECT

8. Stopwatch Design (Top-down) – verification of layout(DRC/ERC)

DRC/ERC the Synthesized/PnR by OpenROAD on ETRI MPW platform, Fix Errors



*Warning
If there is DRC error,
you need to fix it manually.

Before checking ERC,
you need to add VDD and
GND label correctly
to avoid ‘no power connected’
error.

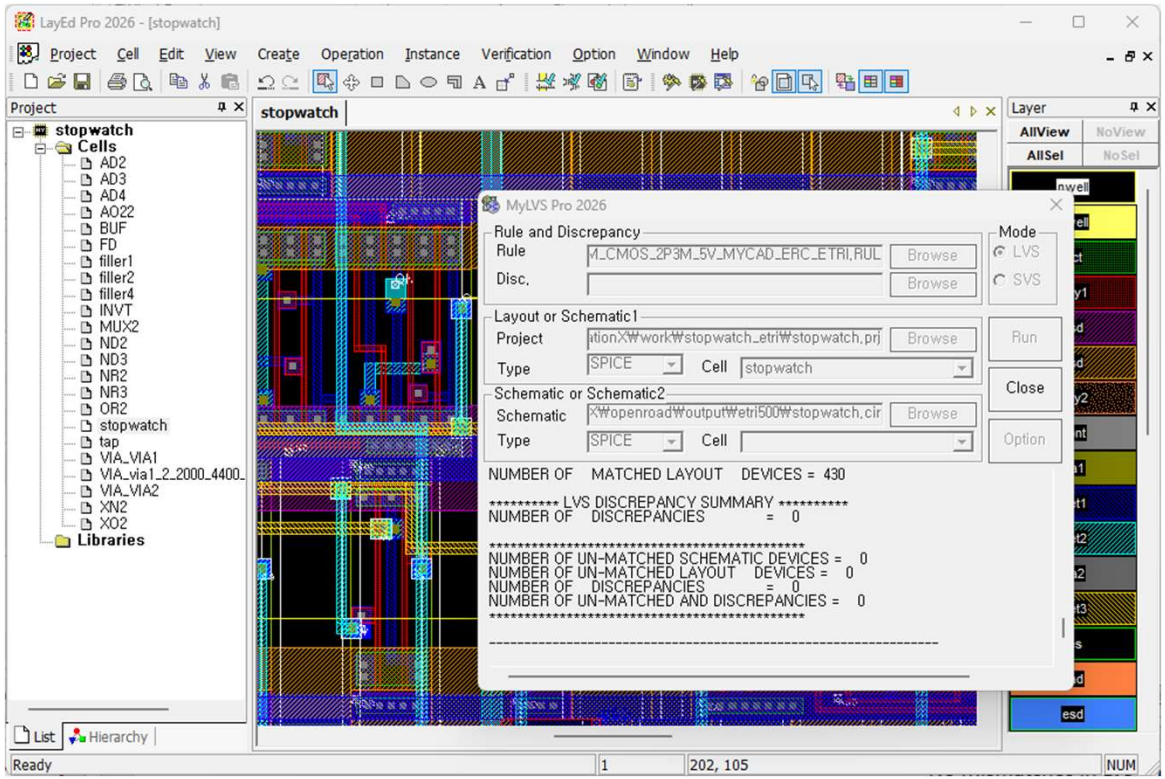
SELCONN
SELECT & CONNECT

8. Stopwatch Design (Top-down) – verification of layout(LVS check)

(CDL → Verilog → Flatten → MOS Extract → Net Rename → Reduce → Compare → LVS Clean)

```
****************************************
***  REDUCE (LAYOUT) SUMMARY REPORT
****************************************
---------- TOTAL LAYOUT DEVICES -----------
MOS     : 852
---------- REDUCED LAYOUT DEVICES ---------
MOS     : 176
INV     : 191
NAND    : 35
NOR     : 25
AOI2    : 3

****************************************
***  REDUCE (SCHEMATIC) SUMMARY REPORT
****************************************
--------- TOTAL SCHEMATIC DEVICES ---------
MOS     : 852
--------- REDUCED SCHEMATIC DEVICES -------
MOS     : 176
INV     : 191
NAND    : 35
NOR     : 25
AOI2    : 3
```

100% logic matches

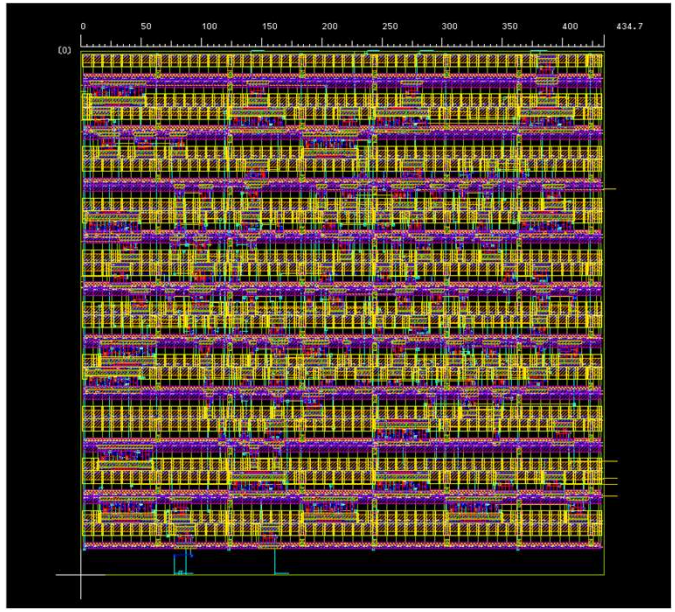


No Mismatches in LVS

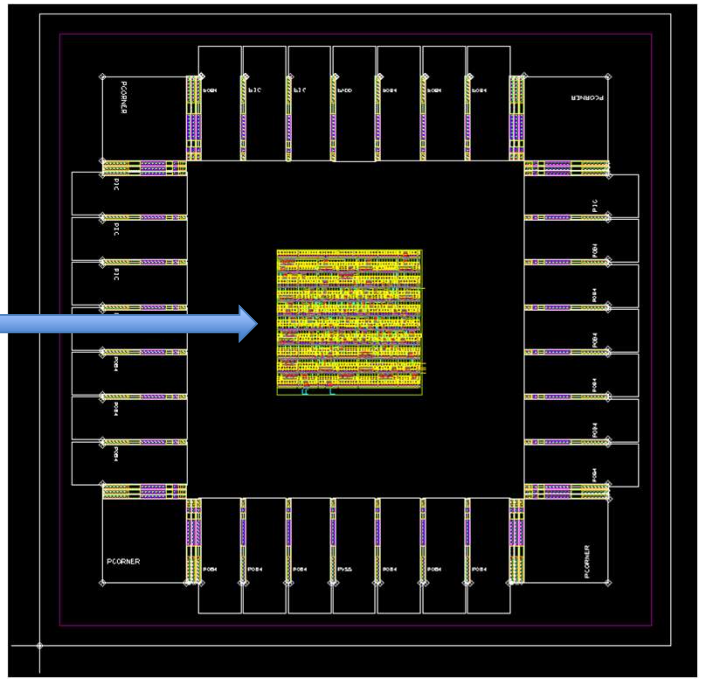
SELCONN
SELECT & CONNECT

8. Stopwatch Design (Top-down) – MPW chip layout on MyChipStationX

Verilog → OpenROAD(Yosis, Openroad, klayout) → Synthsis/Placement/Routing → Import on MyChipStationX -> MyChipStationX(IO/PAD + Stopwatch_core) -> MyChipStationX(DRC, ERC, LVS) -> Tapeout



Synthesized stopwatch core in OpenROAD
Edited and Verified on MyChipStationX



Merged with IO/PAD in MyChipStationX

SELCONN
SELECT & CONNECT

Thank You!