# MyChipStationX Quick Start Guide

**The Complete Windows-Based RTL-to-GDSII Framework**

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# 1. Introduction

Welcome to MyChipStationX.

MyChipStationX provides a complete IC physical design environment on Windows. It integrates:

- Layout Editing
- DRC
- ERC / Extraction
- LVS
- OpenROAD RTL-to-GDSII flow

This Quick Start Guide walks through the shortest path from RTL to a verified layout.

For detailed information, refer to the ‘MyChipStationX User Guide’ and ‘OpenROAD Configuration Guide’ on installed C:\MyChipStationX\Help

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# 2. What You Need

**1. MyChipStationX**

Download MyChipStationX from the Selconn website. You may either:

- use the **10-day Trial Version**, or
- purchase a license and activate the software using the license key supplied by Selconn.

Follow the installation instructions provided on the website.

**2. OpenROAD Environment**

Install the following software:

Windows 10 or Windows 11

WSL (Ubuntu)

Docker Desktop

OpenROAD Docker image (openroad-MyCAD)

The installation procedure is described in the **OpenROAD Configuration Guide**.

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# 3. Overall Design Flow

Verilog RTL

▼

OpenROAD
(Yosys + PnR)

▼

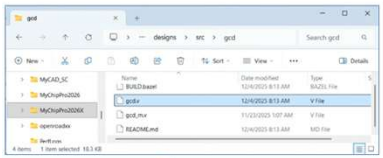
GDSII

▼

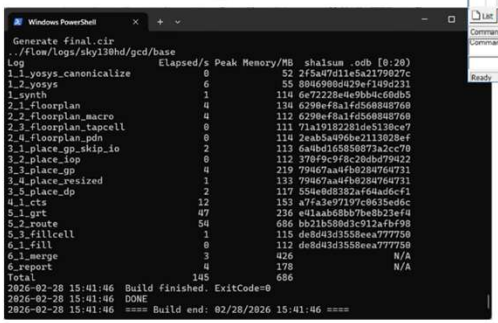
LayEd Pro

- DRC
- ERC / Extraction
- LVS

1. Update Design (Verilog) On Windows

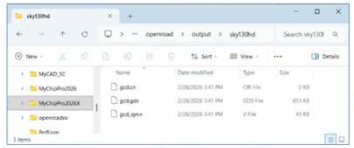


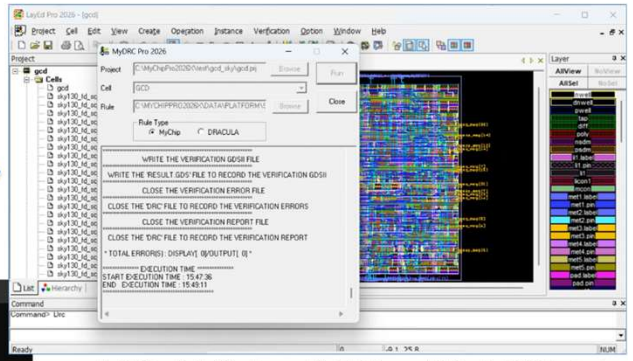

2. Run OpenROAD




3. OepnROAD Processing and results (Synthesis & PnR)

4. Final result(GDS) on Windows






5. Editing & Verification on MyCAD (Layout Editor & DRC Checker)

Refer to OpenROAD Configuration Guide

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# 4. Start OpenROAD

Run Docker Desktop. -> Start the container

Run OpenROAD Launcher

```
C:\MyChipStationX\Bin\MyOpenROAD.exe
```

Select

- Platform
- Design

Press

```
Run-OpenROAD
```

The synthesis and physical design process will begin.


Refer to OpenROAD Configuration Guide

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# 5. Locate the Results

After completion, the following files are generated.

```
output/
   sky130hd/
      design.gds
      design.v
      design.cir
```

These files are automatically copied into the shared Windows folder.

Refer to OpenROAD Configuration Guide

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# 6. Open the Layout

Start

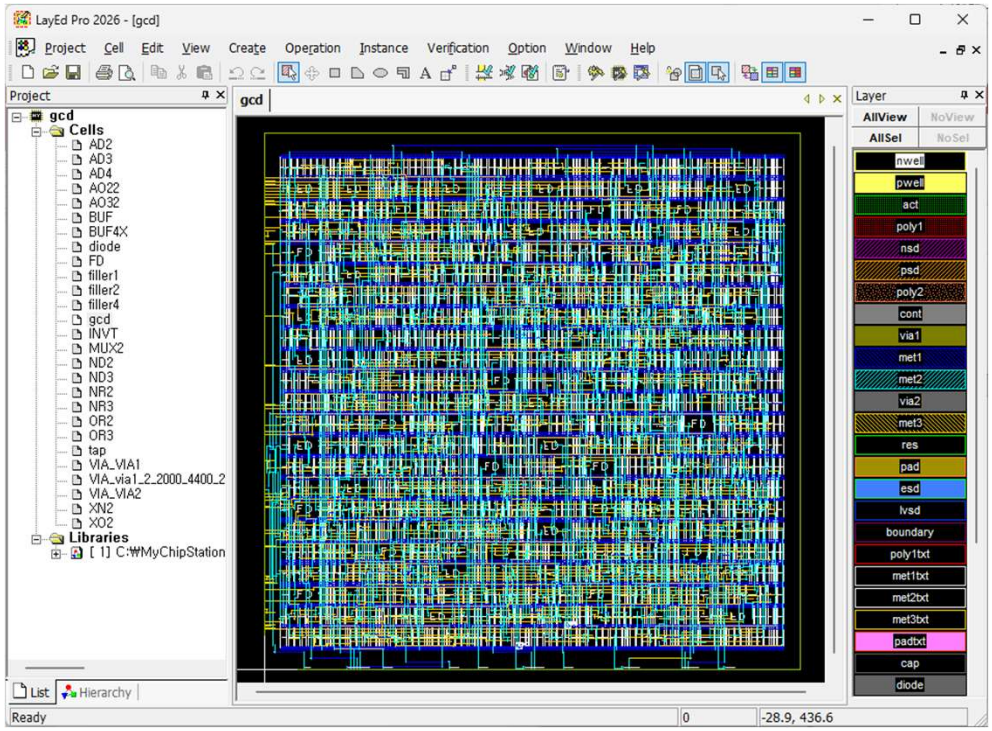
`LayEdPro.exe`

Import

`design.gds`

using the platform technology file.

The routed chip layout is now displayed.




Refer to MyChipStationX User Guide

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# 7. RUN DRC and Fix Layout (Optional)

Choose

Verification

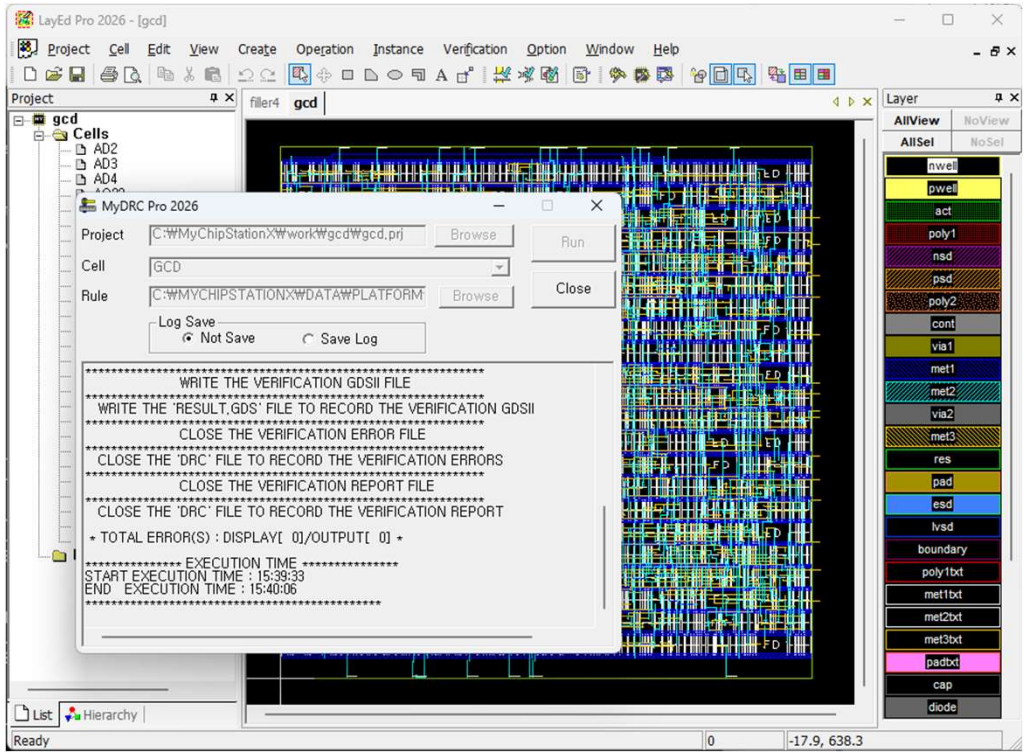
→ DRC

Select the platform DRC rule.

Press

Run

Any violations are automatically displayed in the layout editor.




Refer to MyChipStationX User Guide

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# 8. RUN ERC

Choose

Verification

→ Extract & ERC

The tool

•checks electrical connectivity

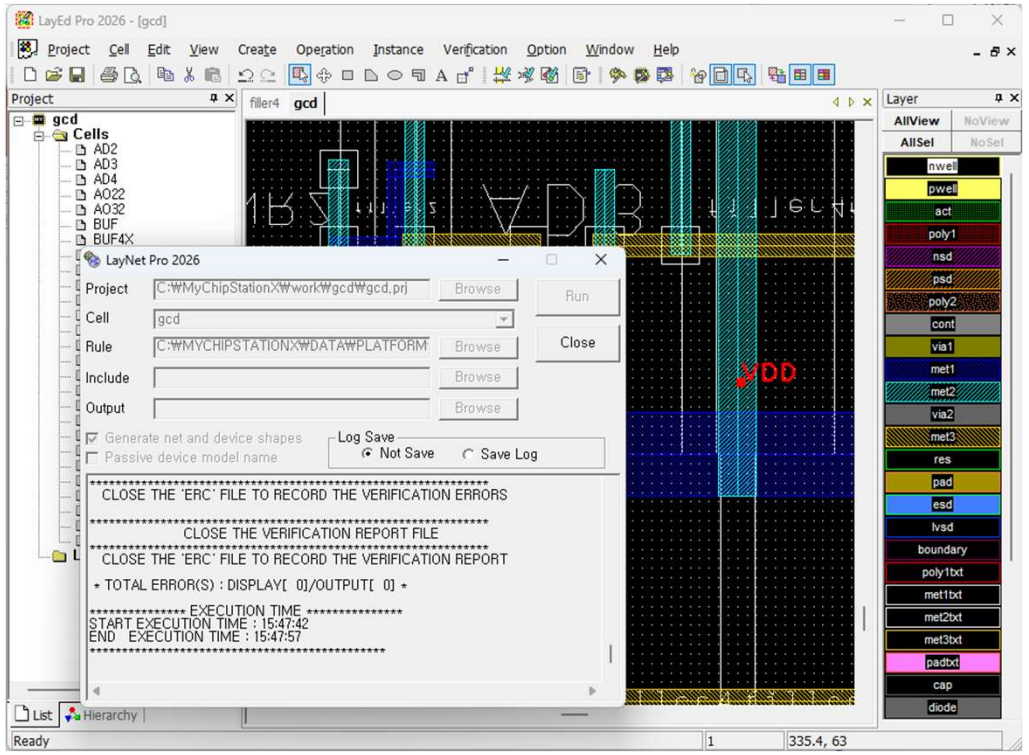
•extracts a SPICE netlist

If required, add

VDD

GND

labels before running ERC.




Refer to MyChipStationX User Guide

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# 9. RUN LVS

Choose

Verification

→ LVS

Use

Design.cir

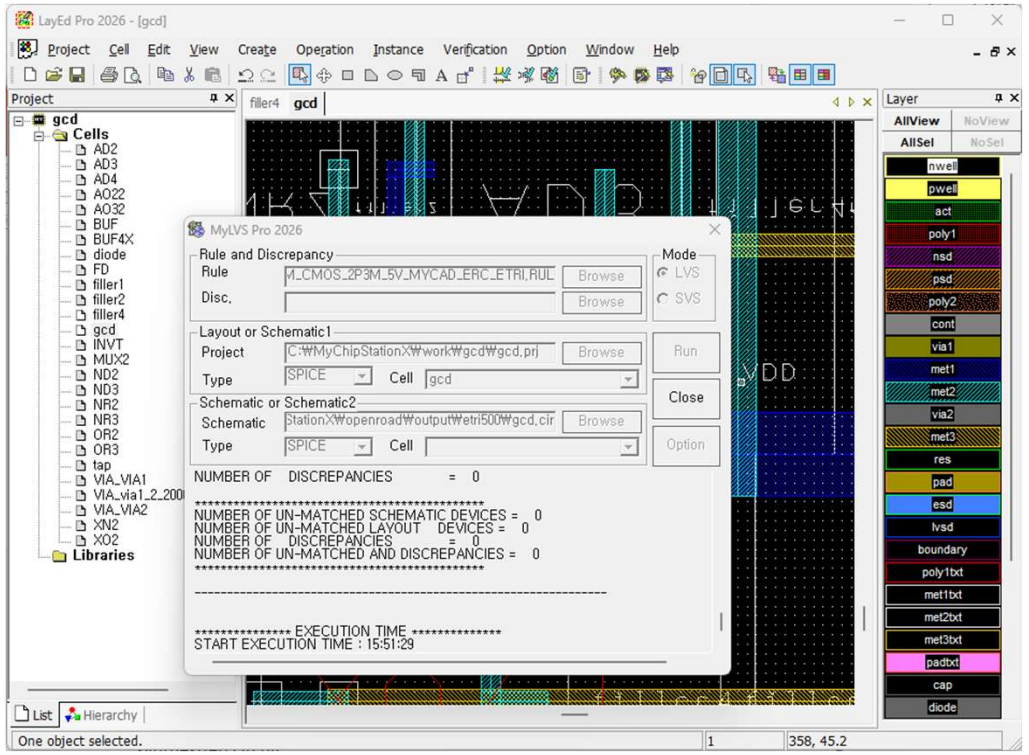
Generated by OpenROAD ad the schematic netlist.

When LVS completes successfully,

`Unmatched is 0`

`Discrepancy is 0`

Indicates that the layout matches the synthesized circuit.




Refer to MyChipStationX User Guide

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# 10. Editing the RTL

RTL files are stored under

```
openroad/
    designs/
        src/
```

Modify the Verilog source and run OpenROAD again.

The updated GDS can then be imported into MyChipStationX.

Refer to OpenROAD Configuration Guide

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# 11. Adding a New Design

Create

```
designs/src/<design_name>/
```

Add

```
design_name.v
```

Create the matching platform configuration.

```
designs/platform/<design_name>/config.mk
```

Run MyOpenROAD again.

Details are described in the OpenROAD Guide.

Refer to OpenROAD Configuration Guide

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# 12. Next Steps

After completing this Quick Start Guide, you can explore:

- Creating projects
- Technology Editor
- Custom layout design
- DRC rule writing
- SPICE extraction
- GDS/CIF translation

using the full **MyChipStationX User Guide**.

Refer to MyChipStationX User Guide

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